PWWHA

Delhi 10R

LA-7202P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)

2011-02-08 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/09/03	Deciphered Date	2012/12/31

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Title: Cover Page		
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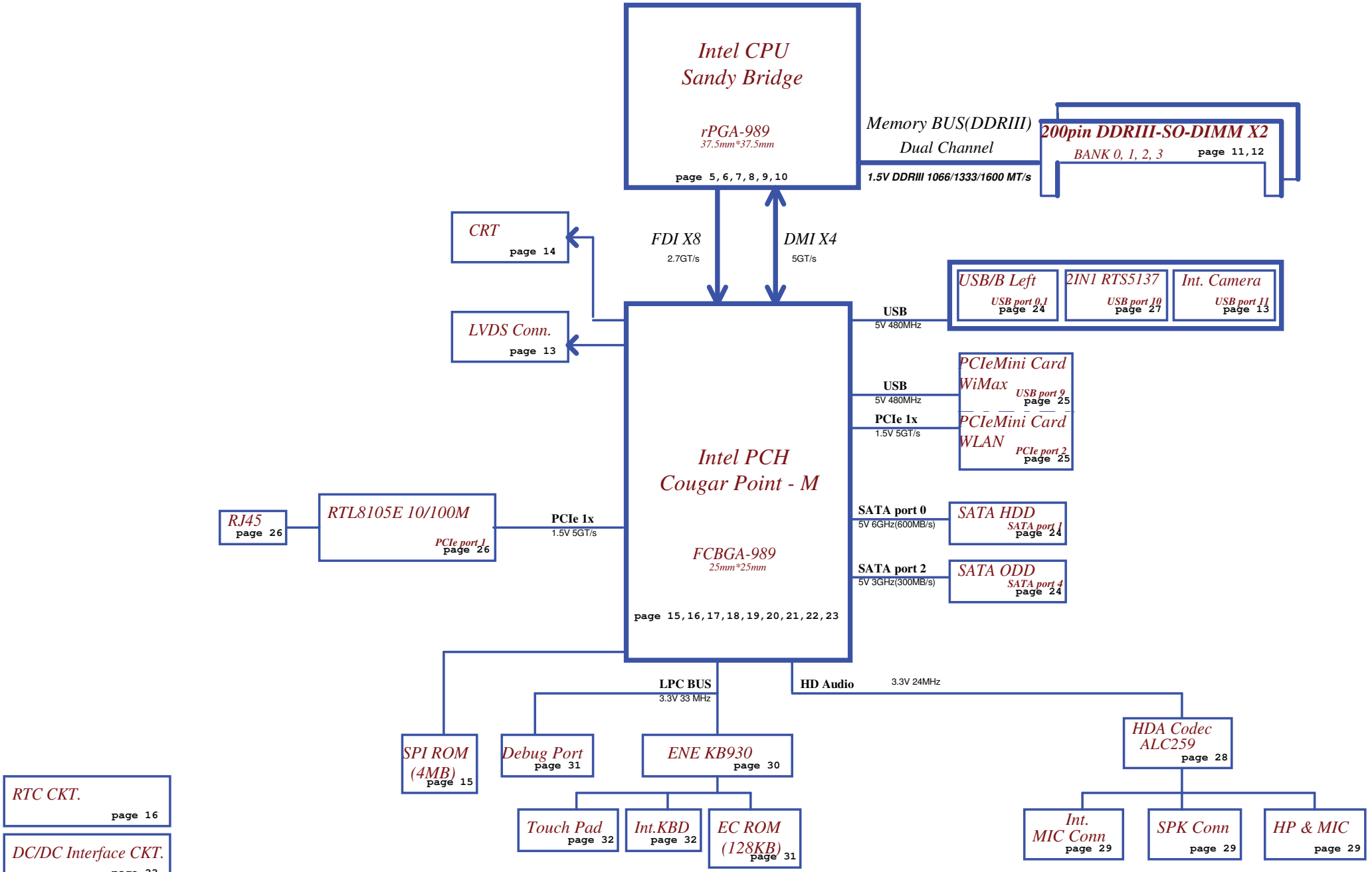

RTC CKT.
page 16

DC/DC Interface CKT.
page 33

Power Circuit DC/DC
page 34,35,36,37,38,39,40,41

Power/B
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Title: Block Diagram		
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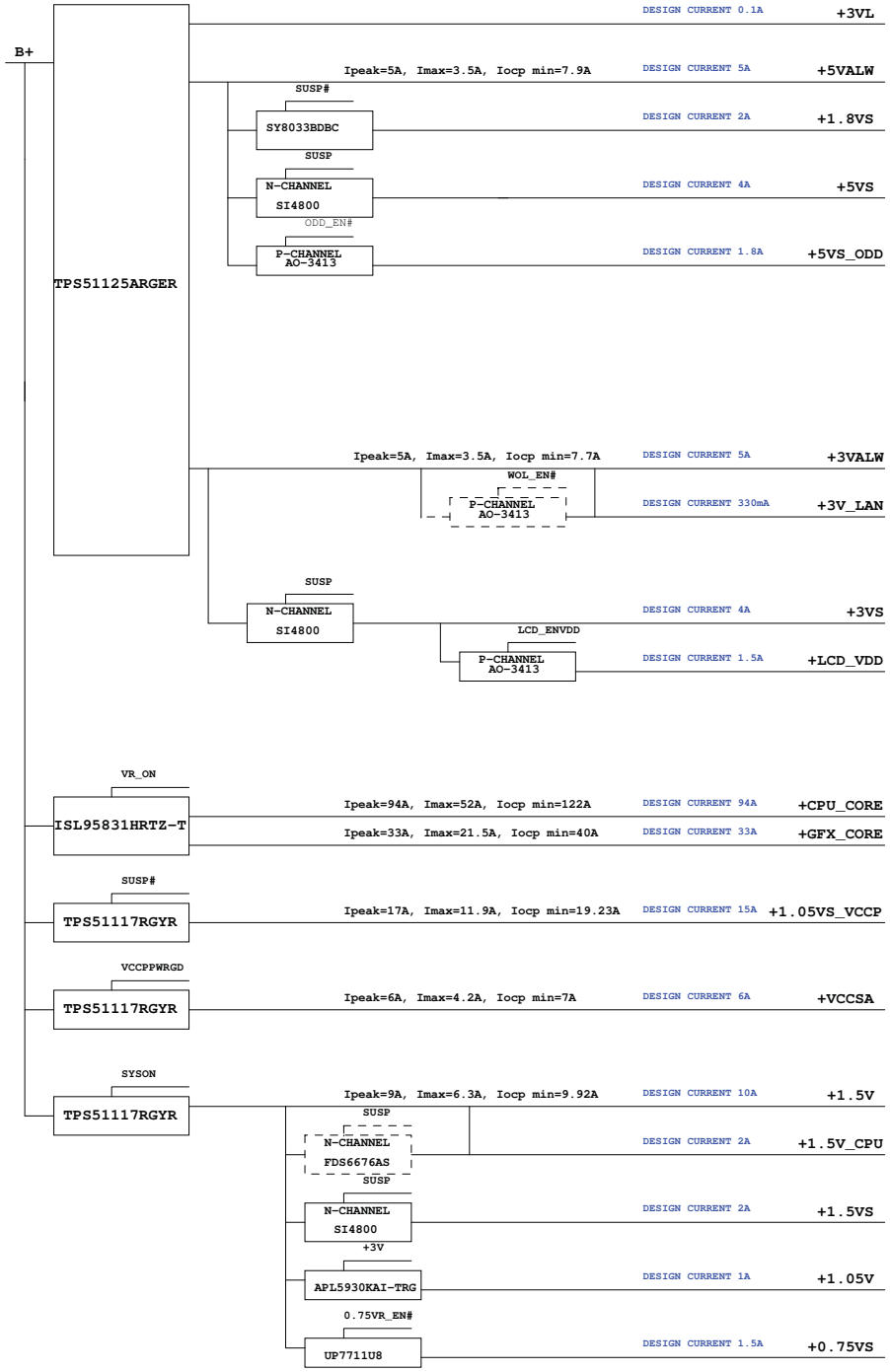

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Title: ***Power Tree***

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	MINI PCI-E SLOT	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
description	SLOT1	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
explain	WIMAX	10/100M	Giga	Camera & Mic	PWM	RPM	1.5V	1.5VS	Old Sch.	New Sch.
BTO	WIMAX@	8105E@	8111E@	CAM@	PWM@	RPM@	WPS3@	PS3@	OLS@	NLS@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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Title: ***Notes List***

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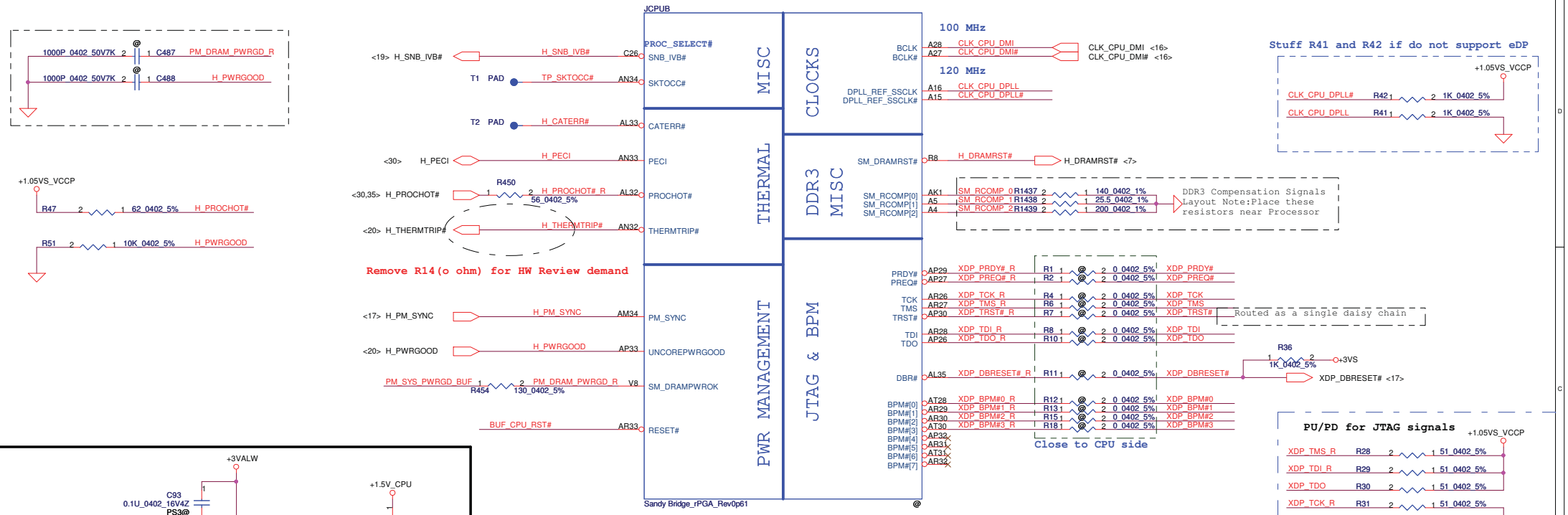

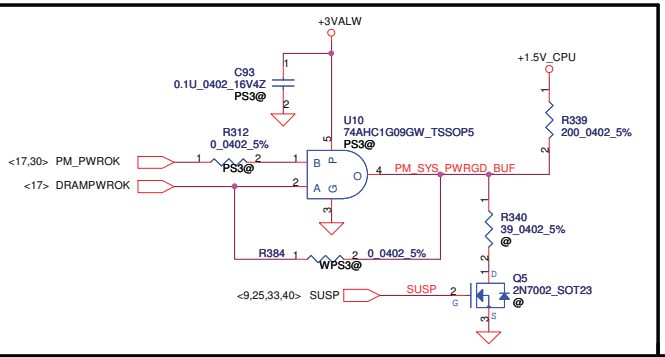

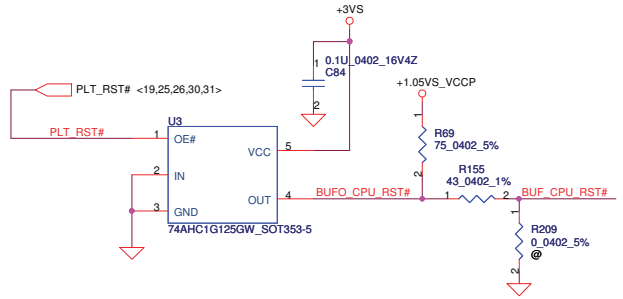

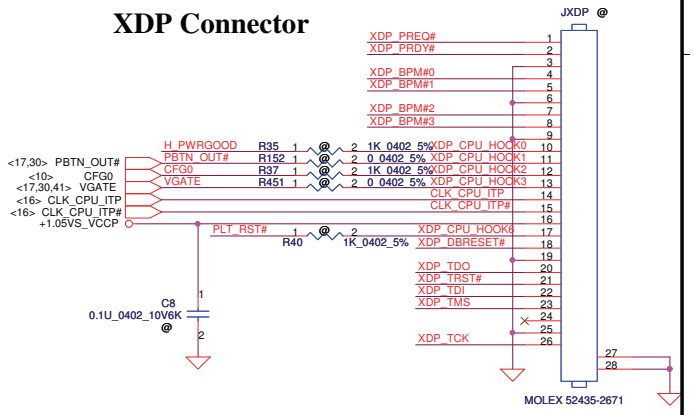

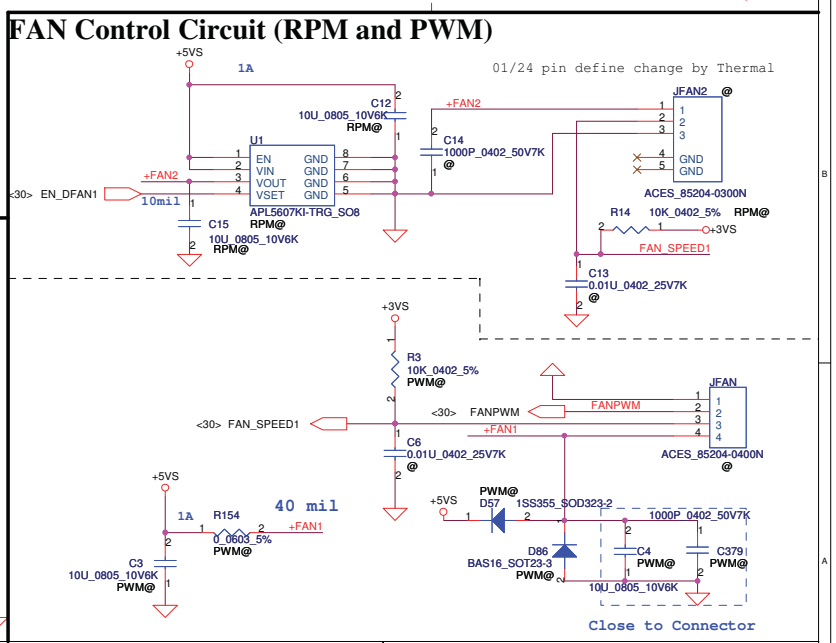

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Title: Sandy Bridge_JTAG/XDP/FAN

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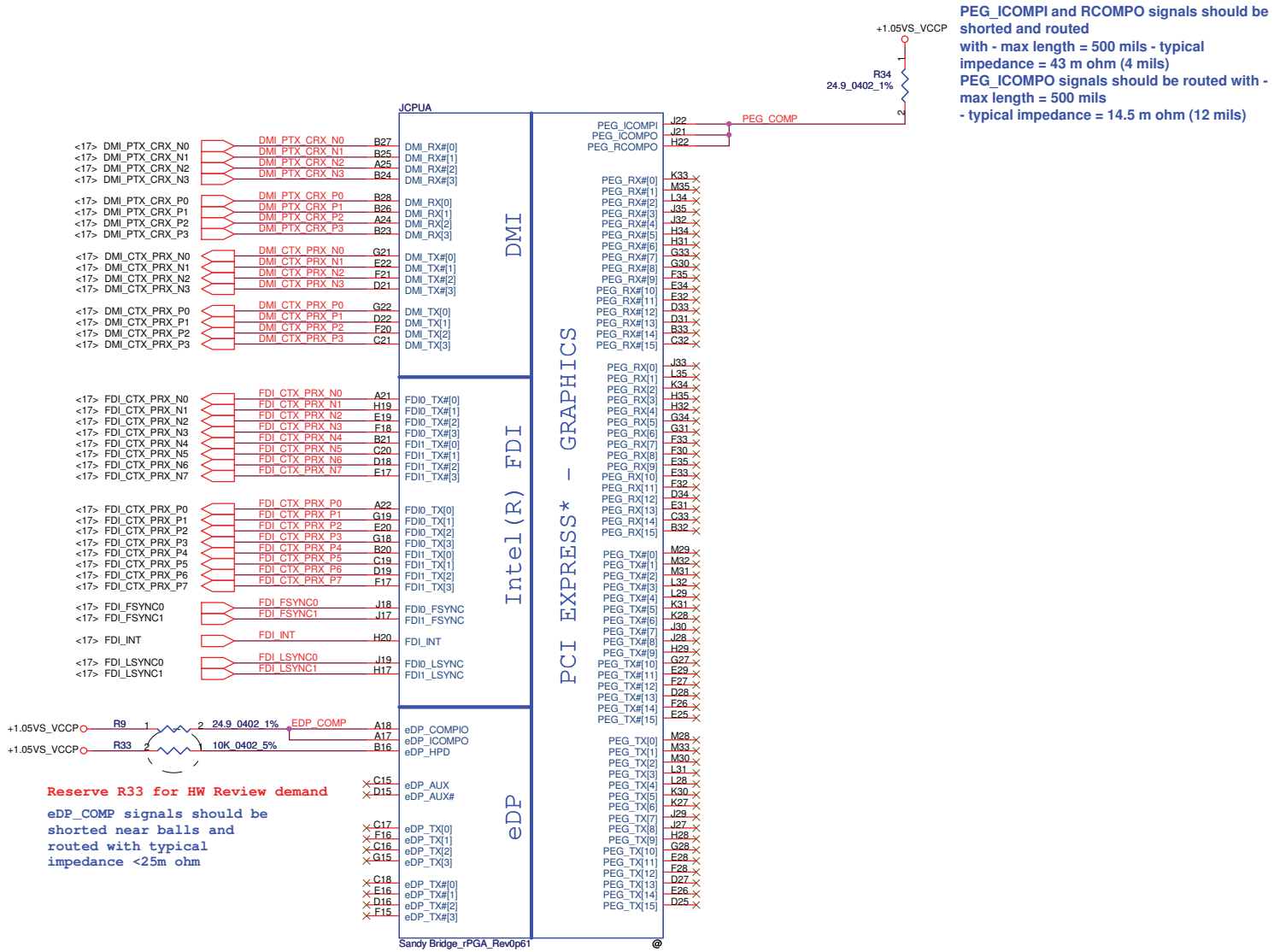

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Title: ***Sandy Bridge_DMI/PEG/FDI***

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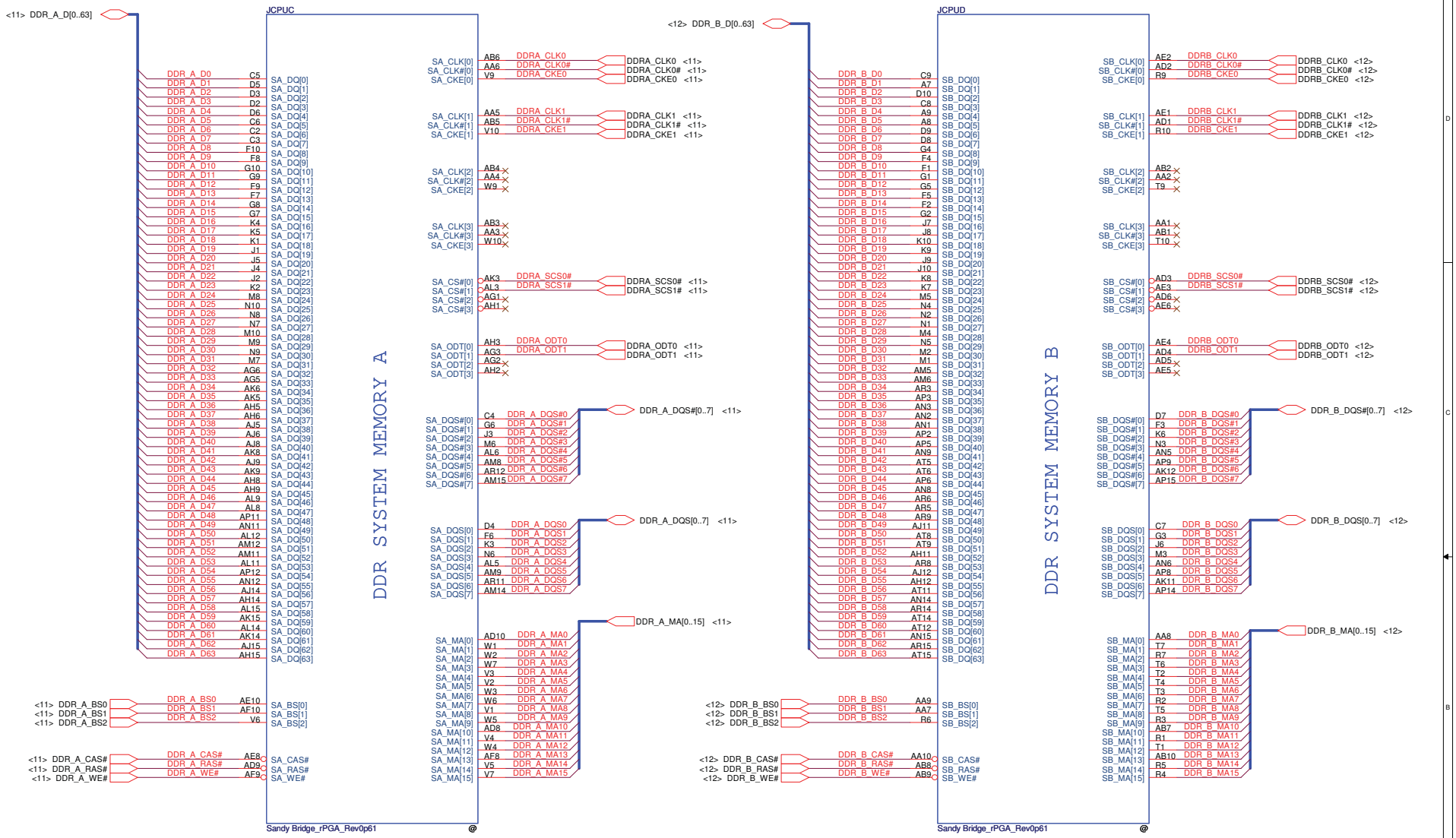

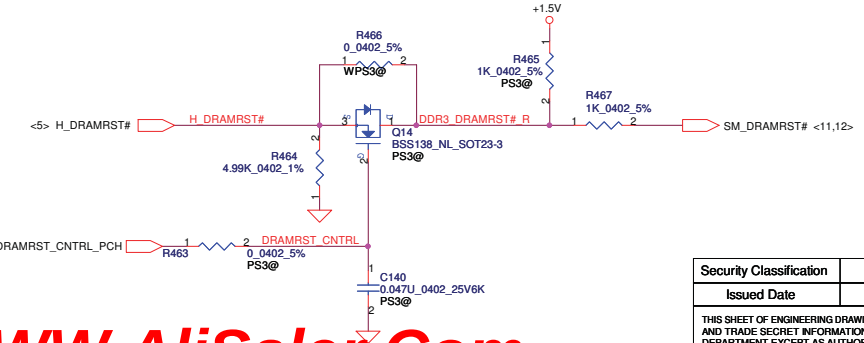

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Title: *Sandy Bridge_DDR3*

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POWER

94A (Quad Core 45W)
53A (SV 35W)

8.5A

+CPU_CORE

JCPUF

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

TOP Socket Cavity x 7

Bottom Socket Cavity x 5

+1.05VS_VCCP

22U_0805_6.3V6M

330U_D2_2V_Y

ESR 9mohm

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

Bottom Socket Cavity

10U_0805_10V6K

Top Socket Edge

Top Socket Cavity

Bottom Socket Edge

330U_D2_2V_Y

R70 130_0402_5%

R68 75_0402_5%

R67 43_0402_1%

R63 0_0402_5%

R66 0_0402_5%

VIDALERT#
VIDSCLK
VIDSOUT

H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT

VR_SVID_ALRT# <41>
VR_SVID_CLK <41>
VR_SVID_DAT <41>

Pull high resistor on VR side

R64 100_0402_1%

R62 100_0402_1%

Close to CPU

VCC_SENSE
VSS_SENSE

VCCSENSE_R
VSSSENSE_R

R65 0_0402_5%
R52 0_0402_5%

VCCSENSE <41>
VSSSENSE <41>

VCCIO_SENSE
VSSIO_SENSE

VSS_SENSE_VCCIO

R102 0_0402_5%

R105 100_0402_1%

VCCIO_SENSE <40>

Close to CPU

Sandy Bridge_rPGA_Rev0p61

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Title: *Sandy Bridge_POWER-1*

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+GFX_CORE Decoupling:
1X 560U (10m ohm), 12X 22U

POWER

Change C873 from 330uF to 560uF for power issue

Bottom Socket Edge

Bottom Socket Cavity

Top Socket Cavity

Top Socket Edge

JCPUG

33A

SENSE LINES

VREF

GRAPHICS

DDR3 -1.5V RAILS

5A

SA RAIL

6A

MISC

1.8V RAIL

1.2A

Close to CPU

IF PS3@, short PJ32.

+V_SM_VREF should
have 20 mil trace width

+1.5V_CPU Decoupling:
1X 330U (17m ohm), 6X 10U

+VCCSA Decoupling:
1X 330U (17m ohm), 4X 10U

VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2x1U

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge

IF WPS3@, short PJ30.

Vgs=10V, Id=14.5A, Rds=6mohm

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Title: Sandy Bridge_POWER-2

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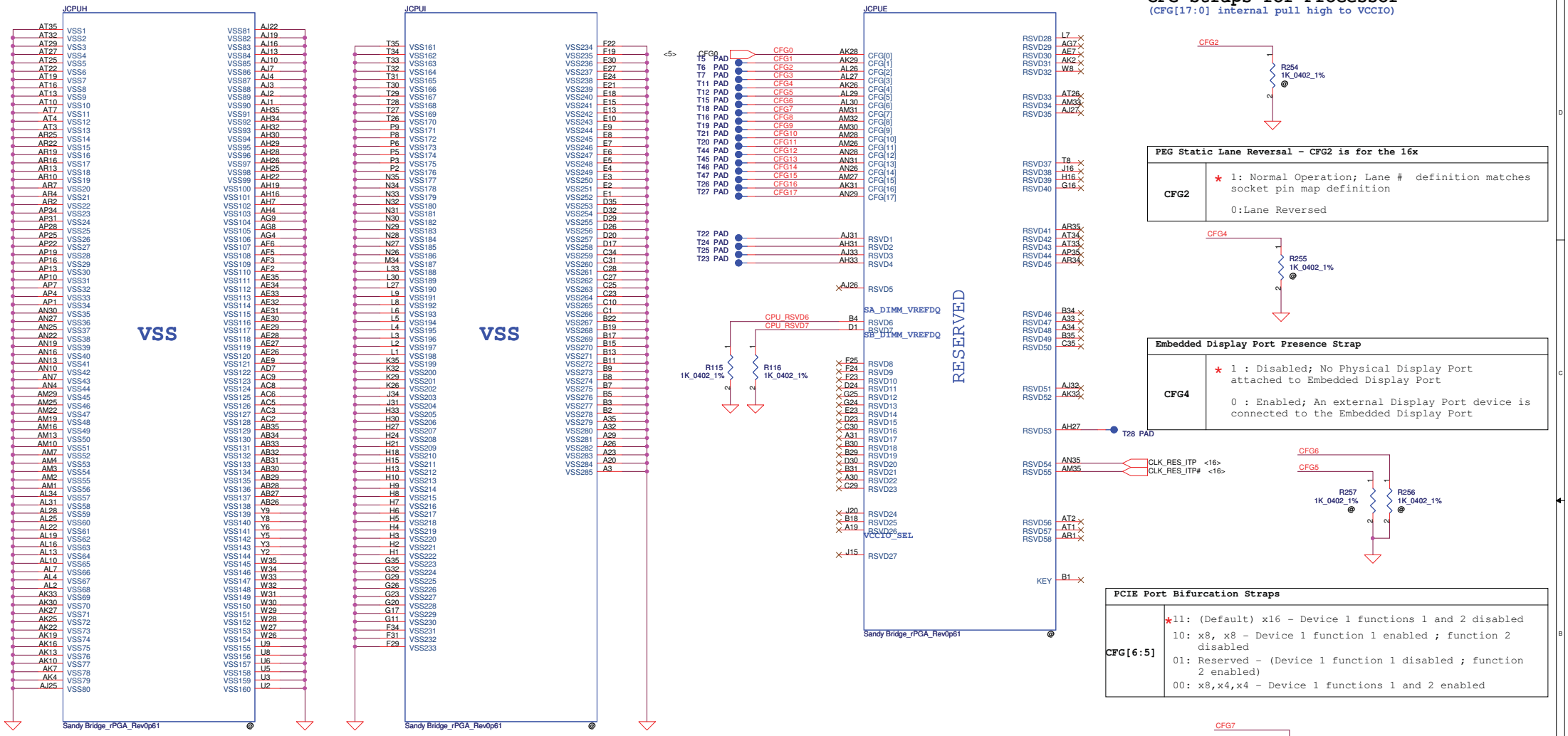

CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)

R254 1K_0402_1% @ — CFG2

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

R255 1K_0402_1% @ — CFG4

Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

RSVD53 — AH27 — T28 PAD

RSVD54 — AN35 — CLK_RES_ITP <16>

RSVD55 — AM35 — CLK_RES_ITP# <16>

R257 1K_0402_1% @ — CFG6

R256 1K_0402_1% @ — CFG5

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

R258 1K_0402_1% @ — CFG7

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: *Sandy Bridge_GND/RSVD/CFG*

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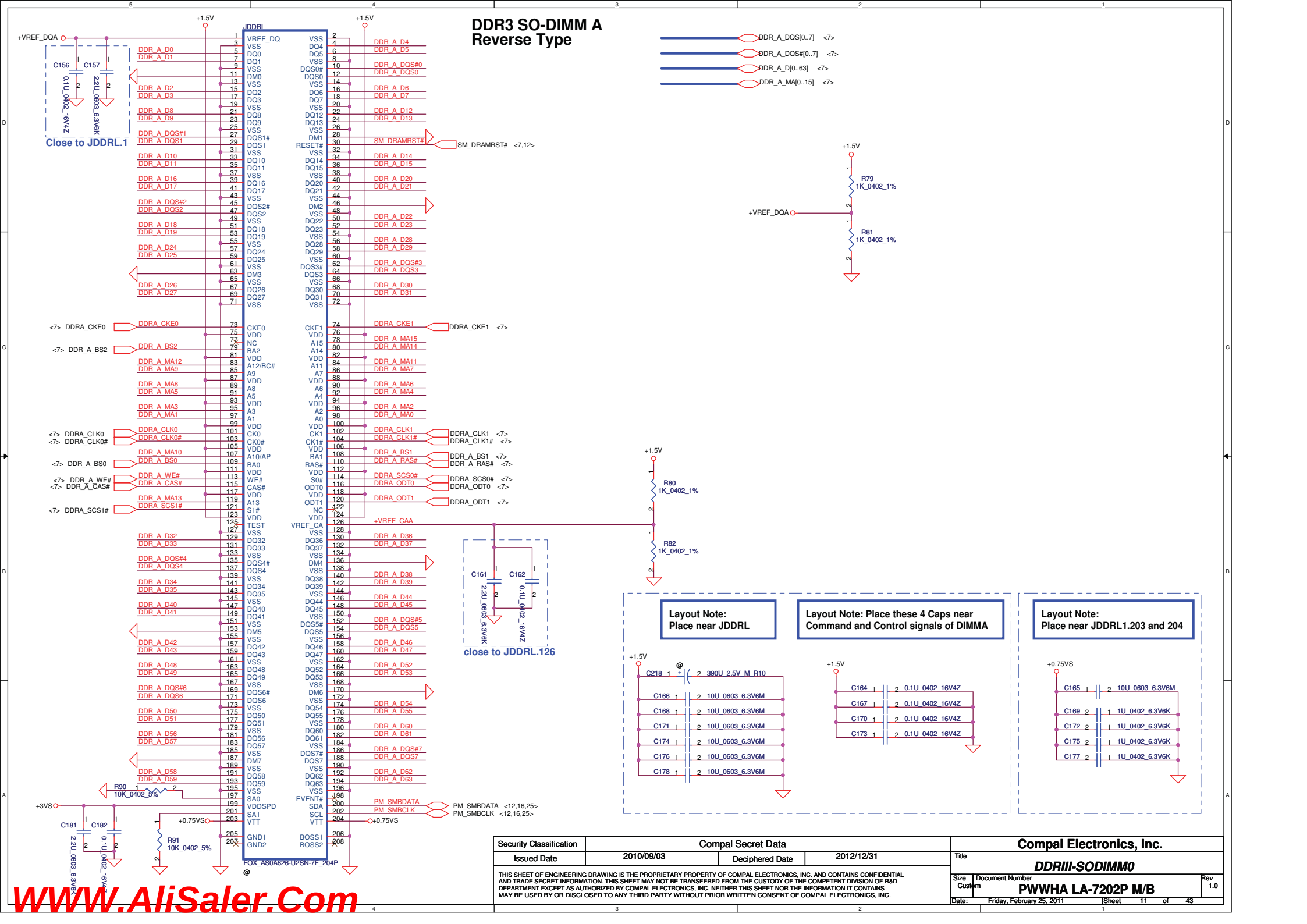
DDR3 SO-DIMM A
Reverse Type



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Title: ***DDRIII-SODIMM0***

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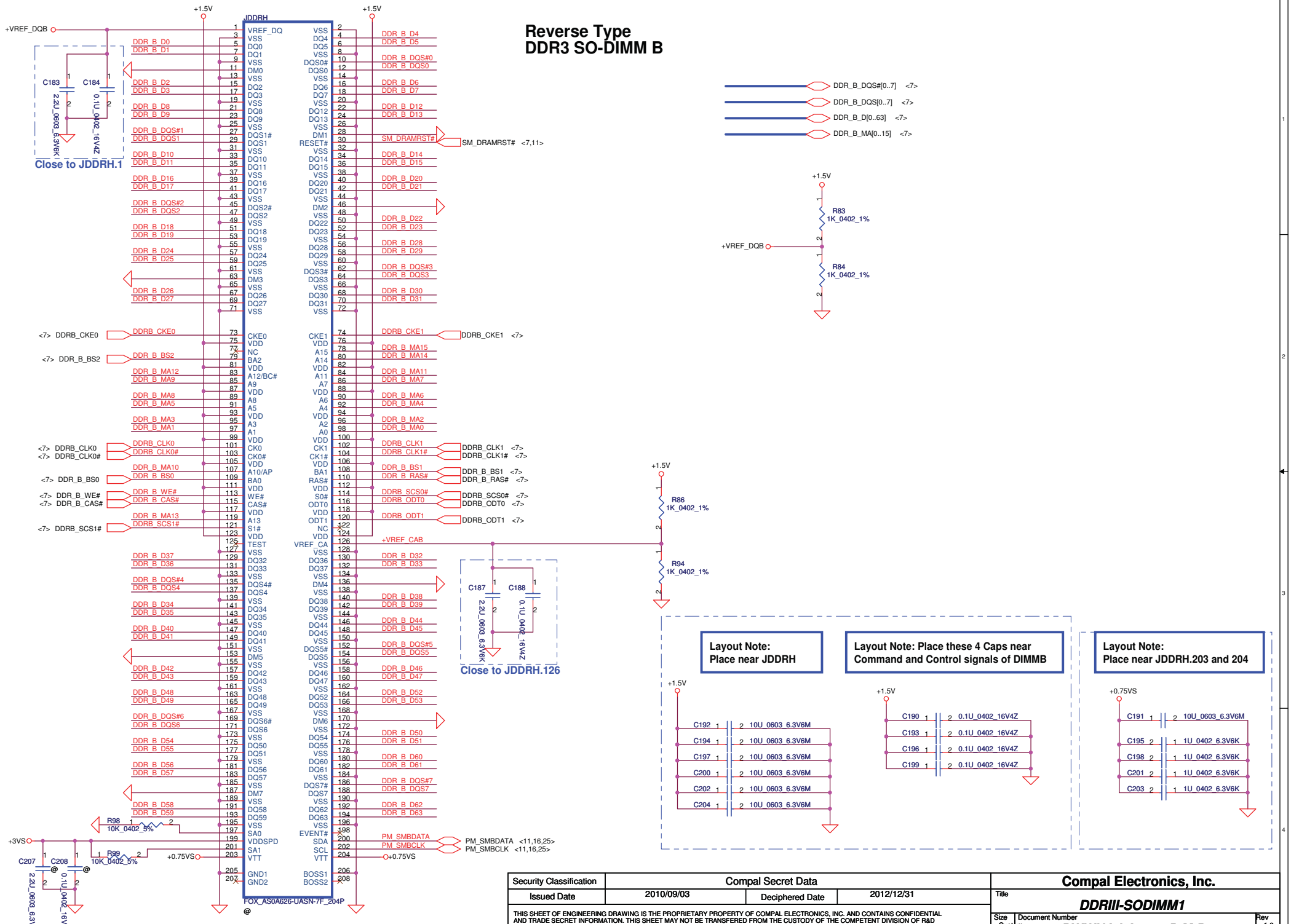
Reverse Type
DDR3 SO-DIMM B



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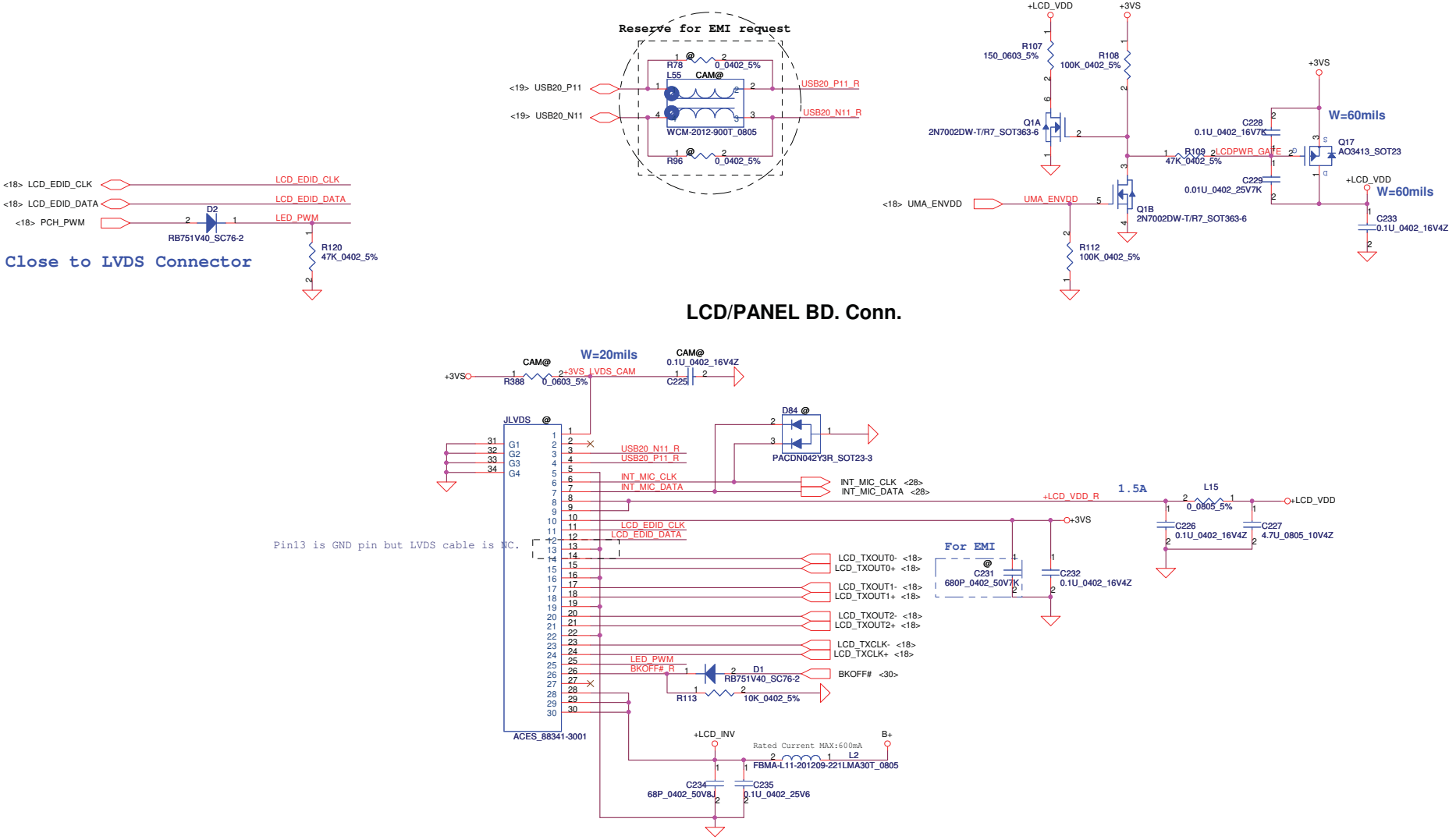

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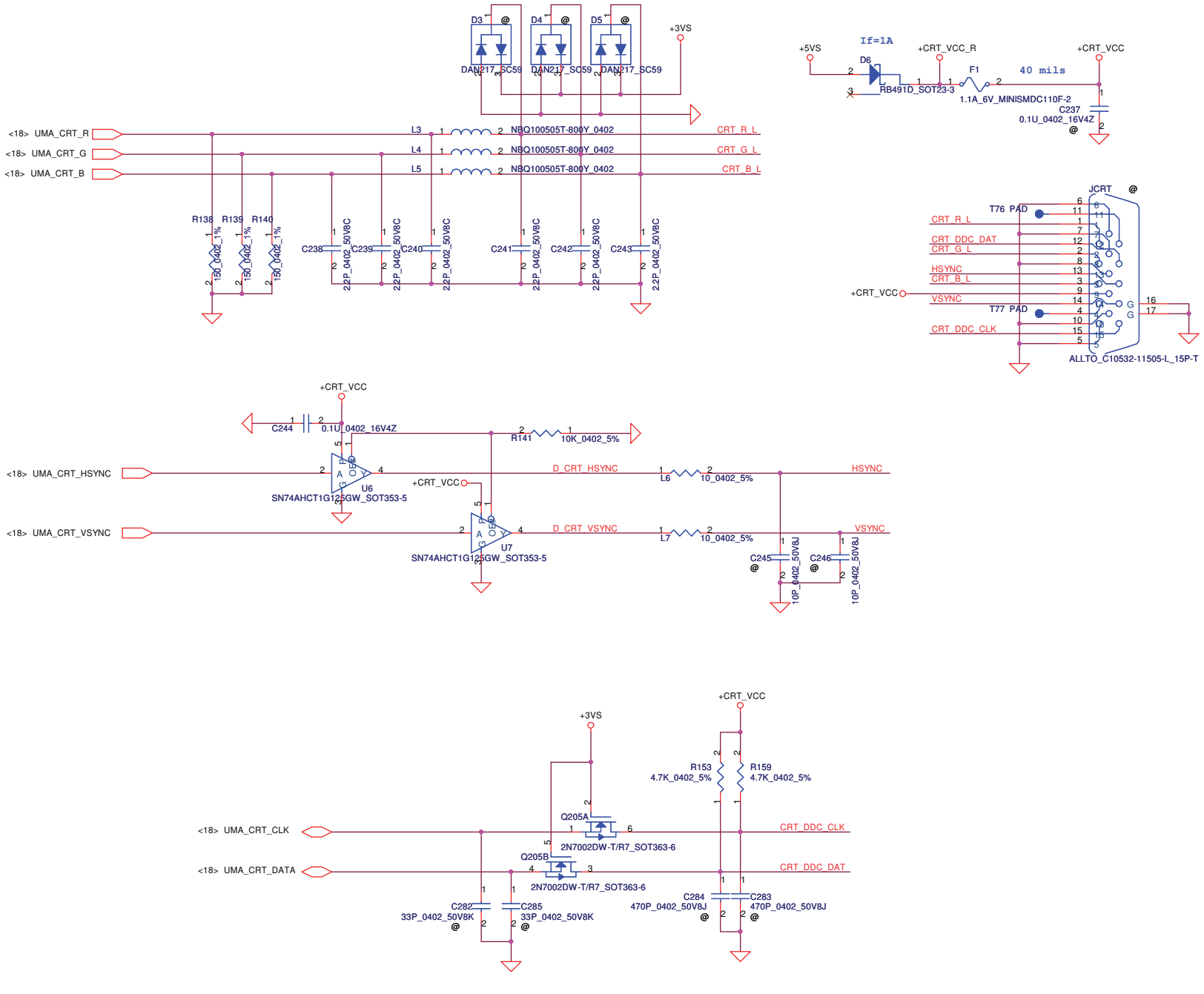
CRT CONNECTOR



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CMOS Setting, near DDR Door

iME Setting.

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

PCH_SPK
High = Enabled (No Reboot)
Low = Disabled (Default)

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

SA000041P00
4M Byte

remove socket for DVT phase, due to ME height limitation
Please close to U2 PCH

for EMI

HDD

ODD

BOOT BIOS Strap Bit 0

RTC schematic for non-chargeable

0812 -> Add R277 for RTC reserve charge

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Title: PCH_HDA/JTAG/SATA/SPI/LPC

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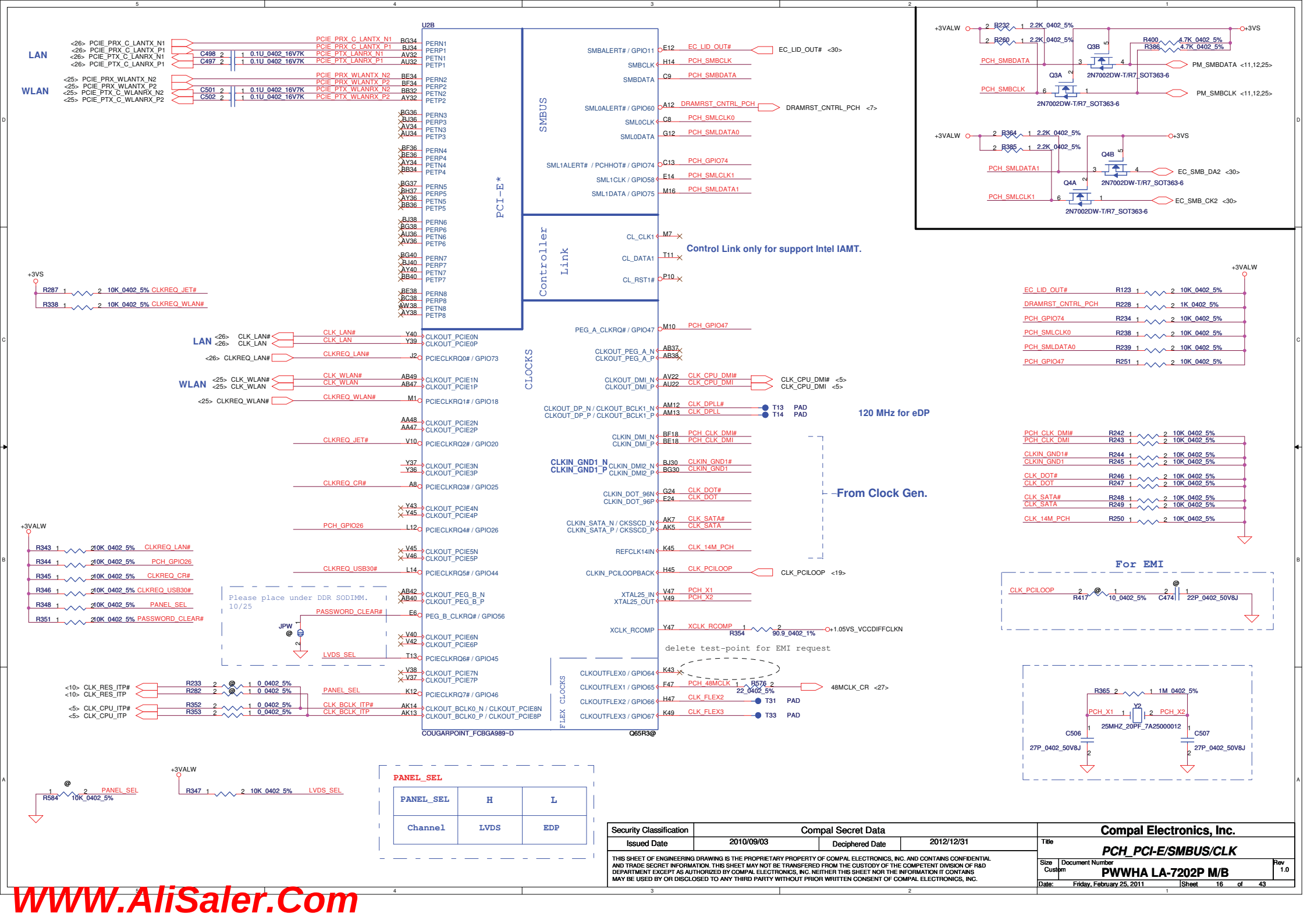

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Compal Electronics, Inc.

Title: PCH_PCI-E/SMBUS/CLK

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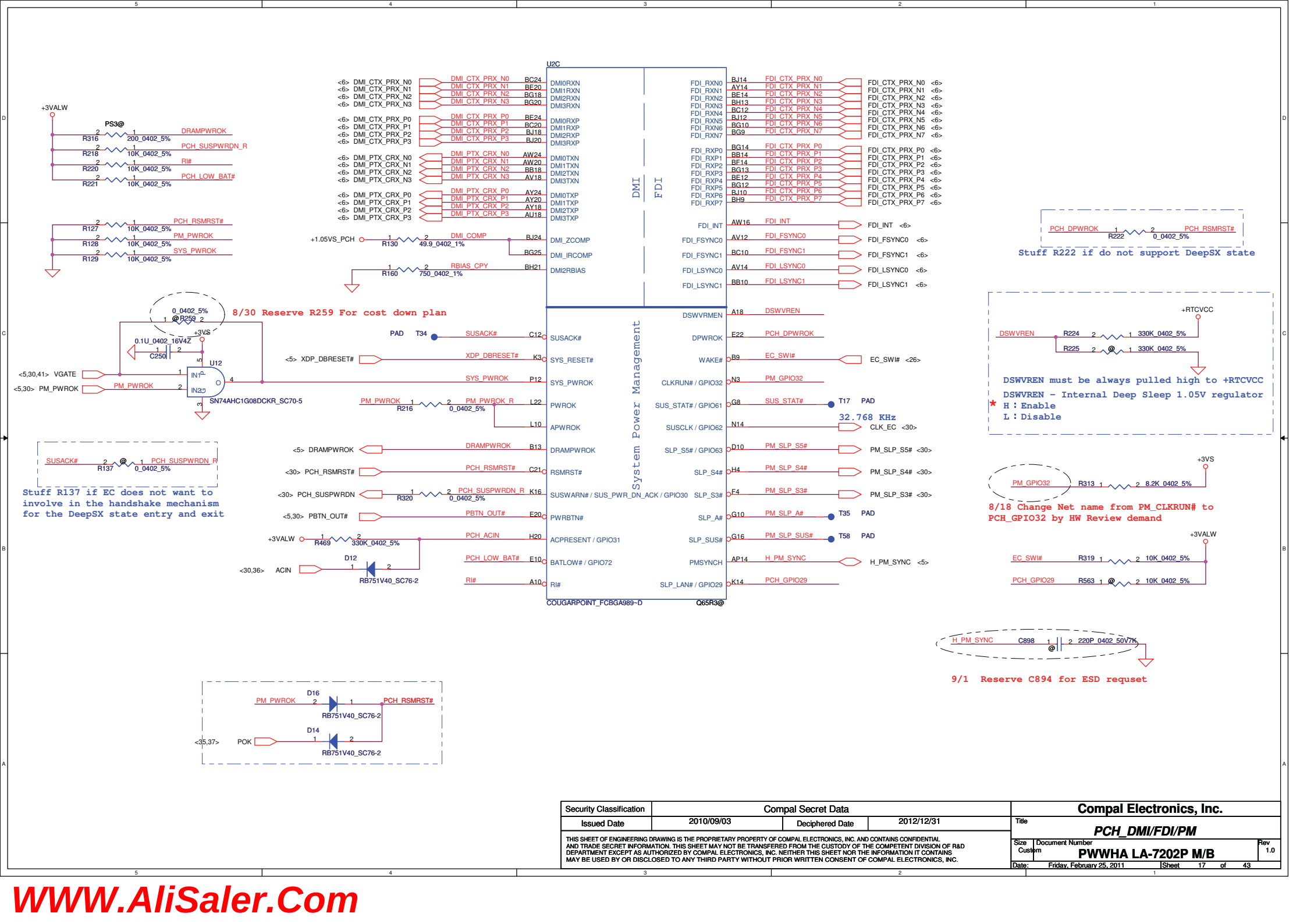

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Compal Electronics, Inc.

Title: *PCH_DMI/FDI/PM*

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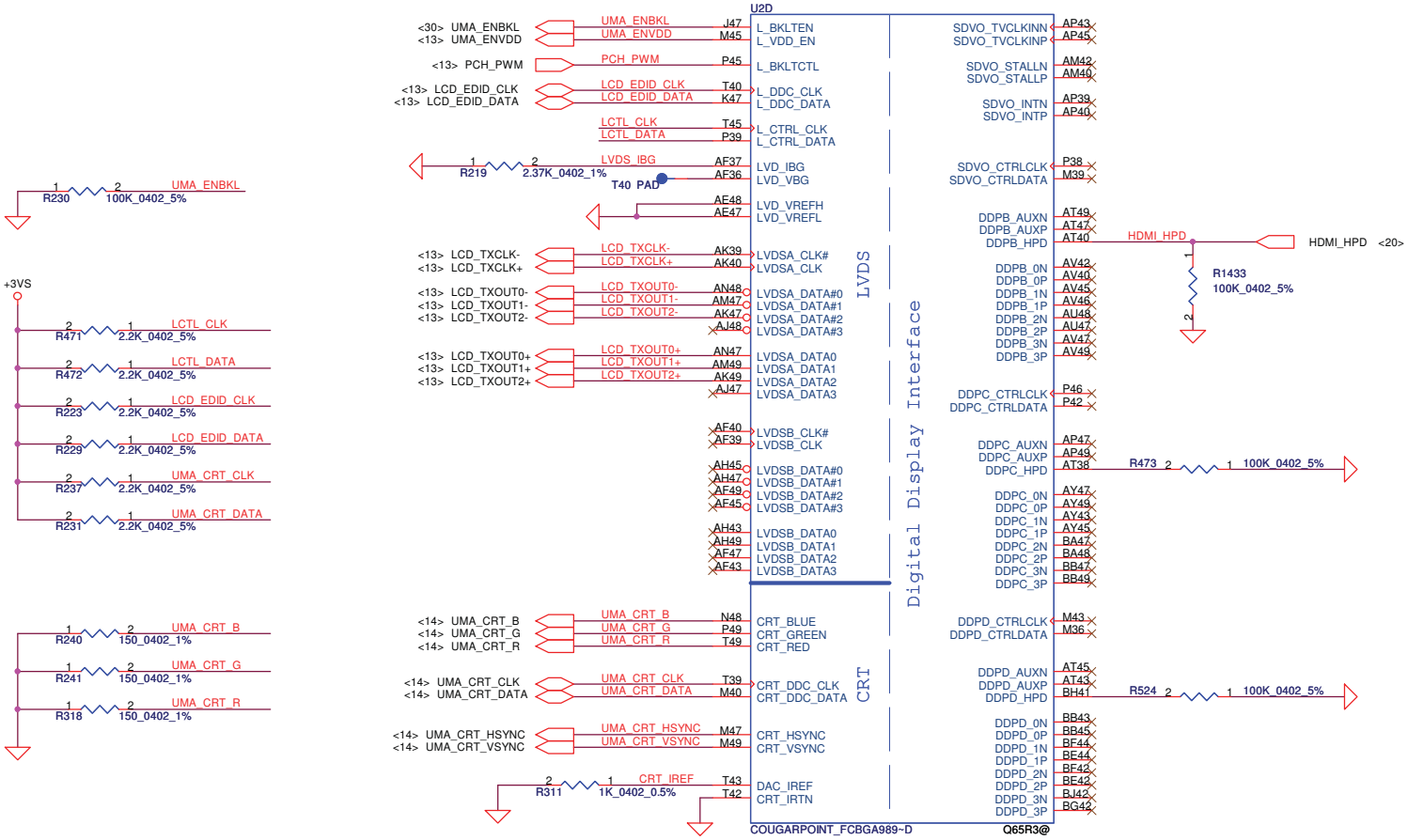

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Compal Electronics, Inc.

Title: ***PCH_CRT/LVDS***

Size	Document Number	Rev
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Date: Friday, February 25, 2011 Sheet 18 of 43

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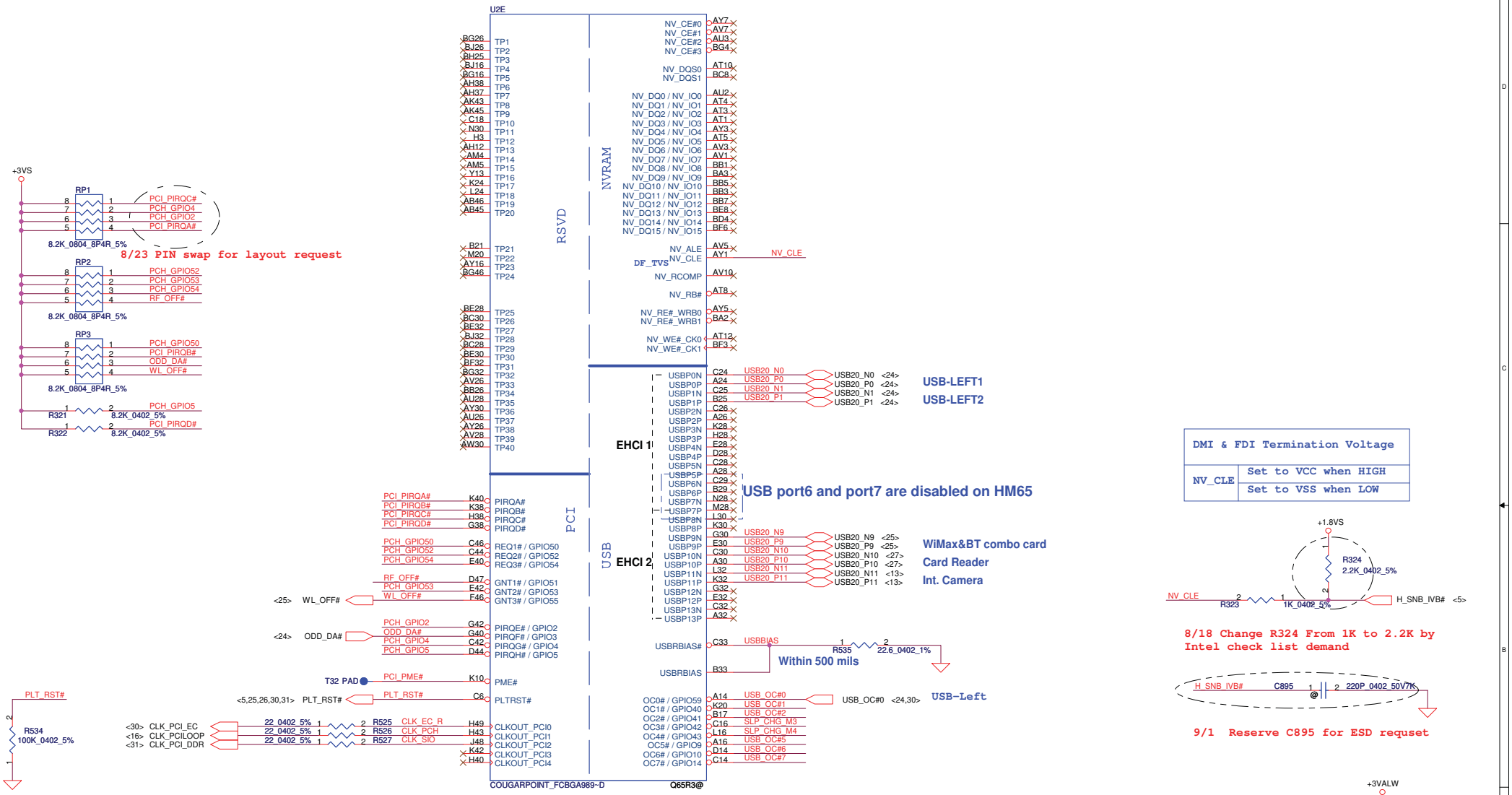

Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

A16 Swap Override Strap	
WL_OFF#	★ Low= A16 swap override Enable High= A16 swap override Disable

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Compal Electronics, Inc.

Title: *PCH_PCI/USB/NAND*

Size	Document Number	Rev
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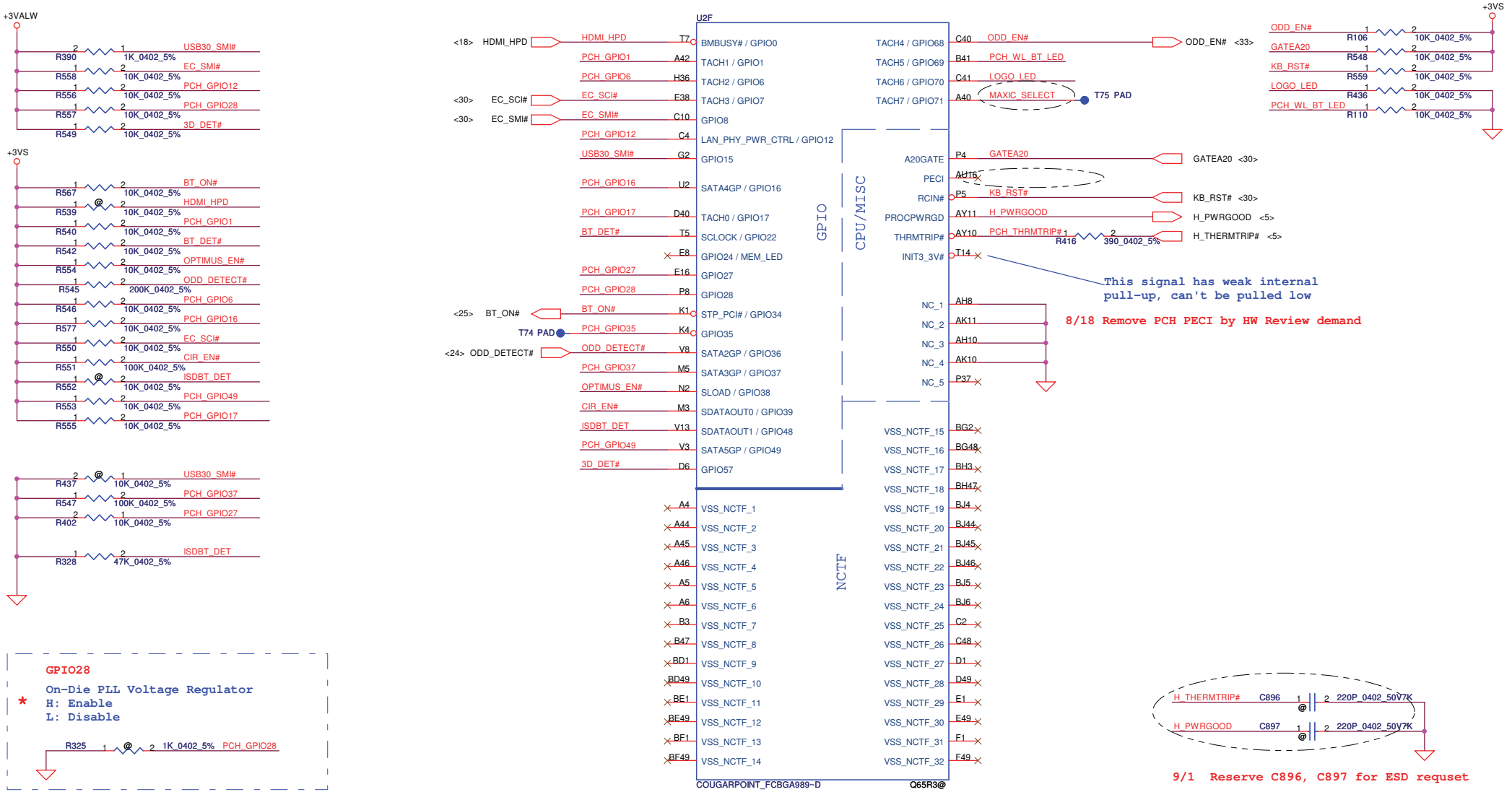
Date: Friday, February 25, 2011 | Sheet 19 of 43



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Compal Electronics, Inc.			
Title	PCH_CPU/GPIO		
Size B	Document Number PWWHA LA-7202P M/B		Rev 1.0
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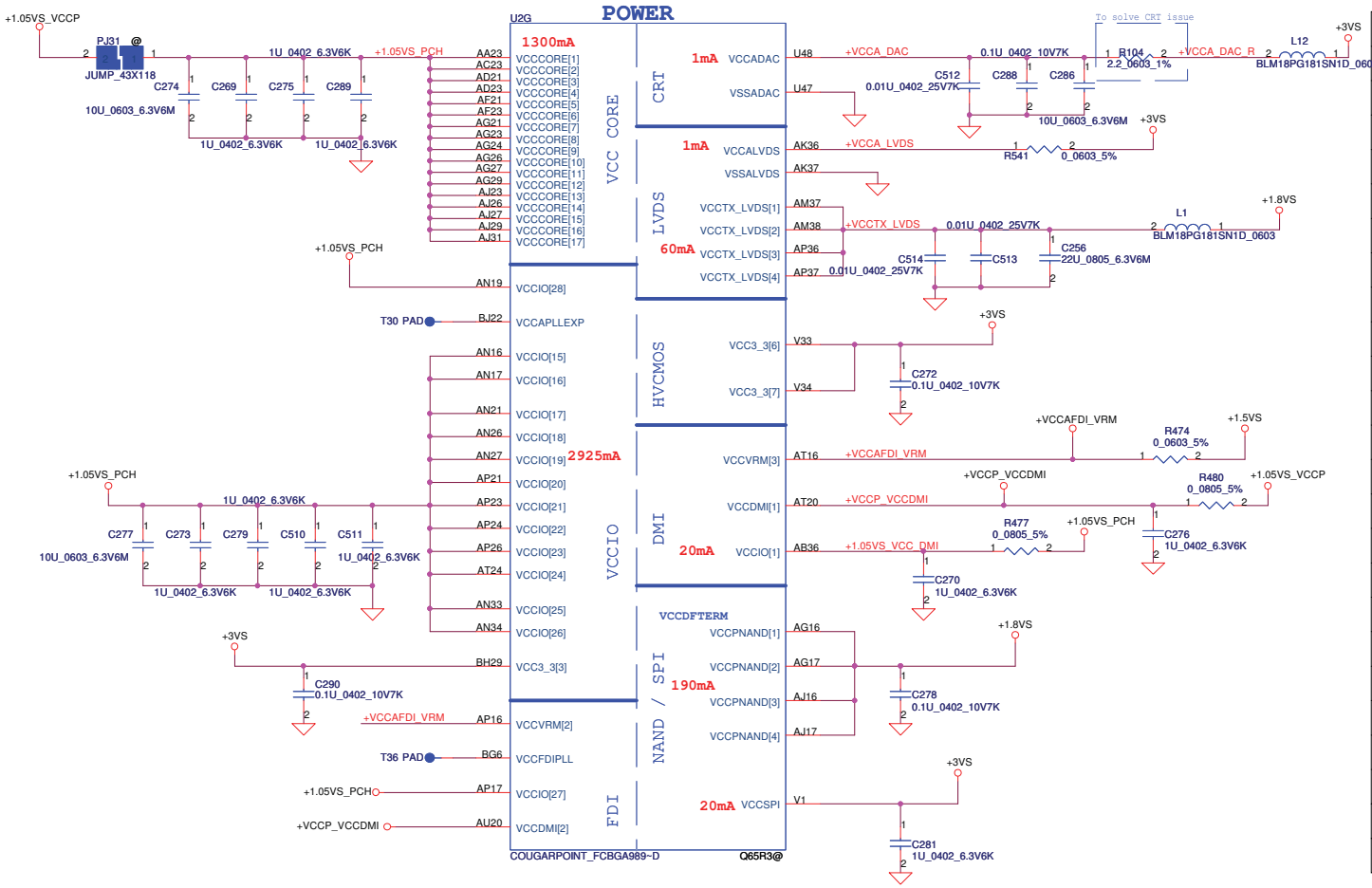

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSusHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

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Compal Electronics, Inc.

Title: *PCH_POWER-1*

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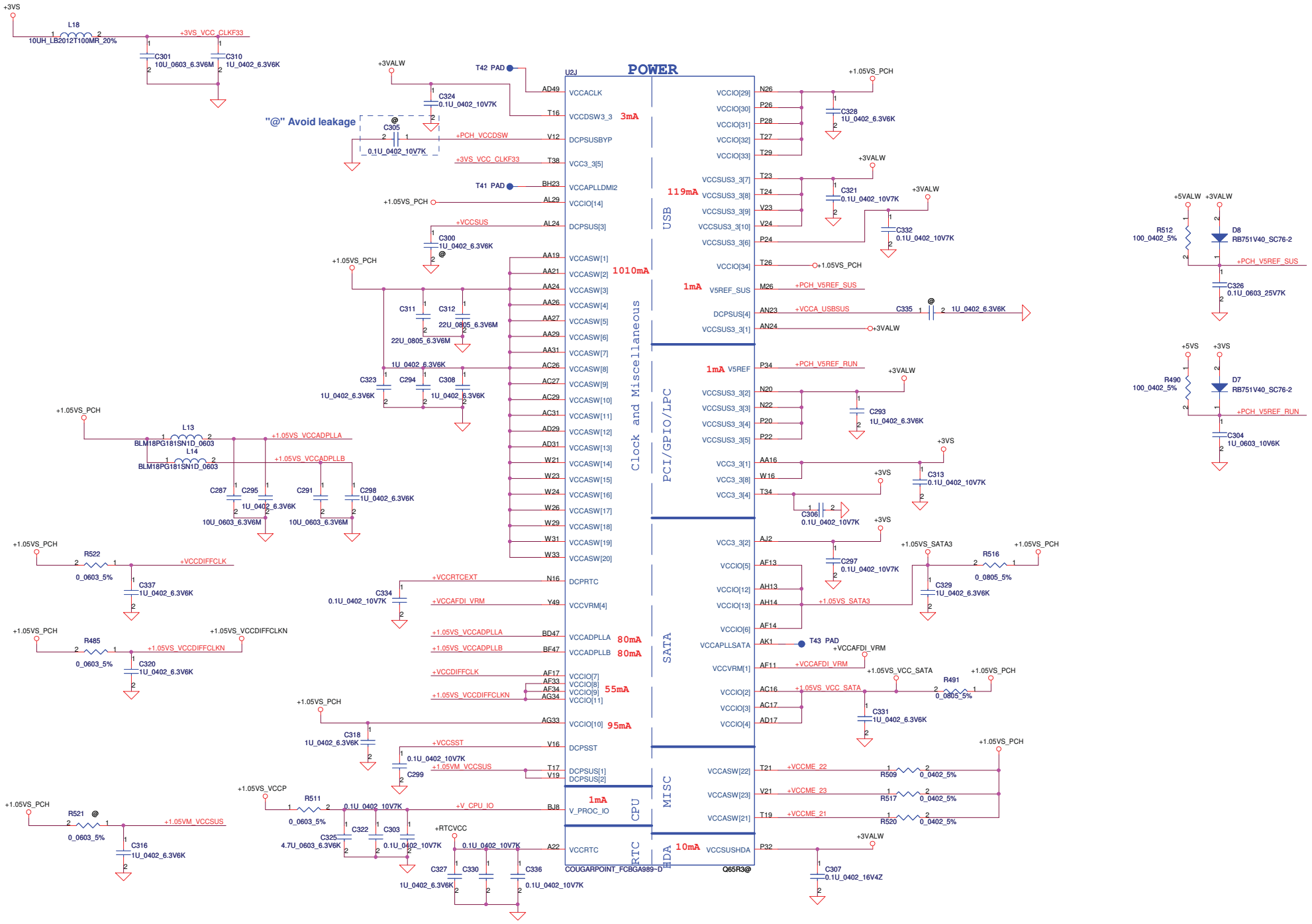

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Compal Electronics, Inc.

Title: ***PCH_POWER-2***

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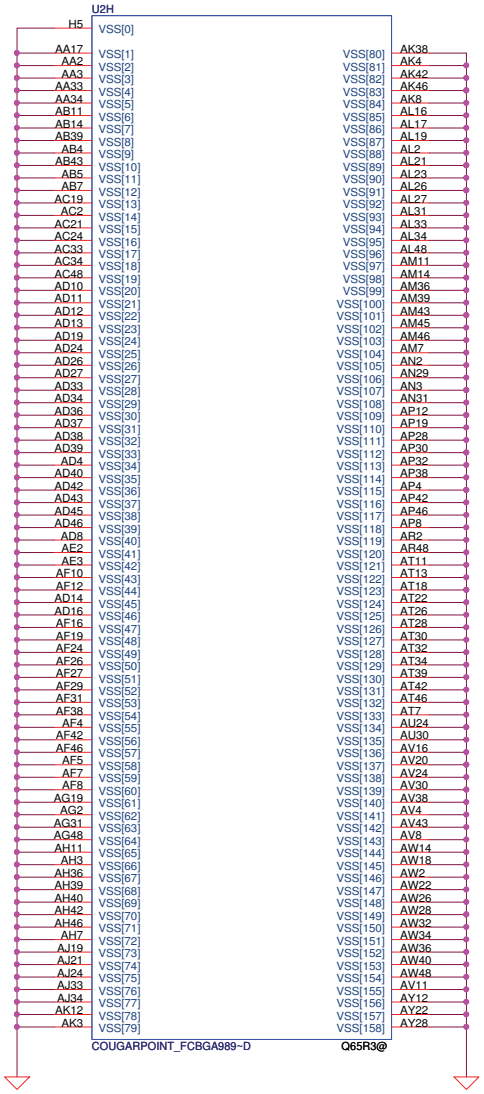

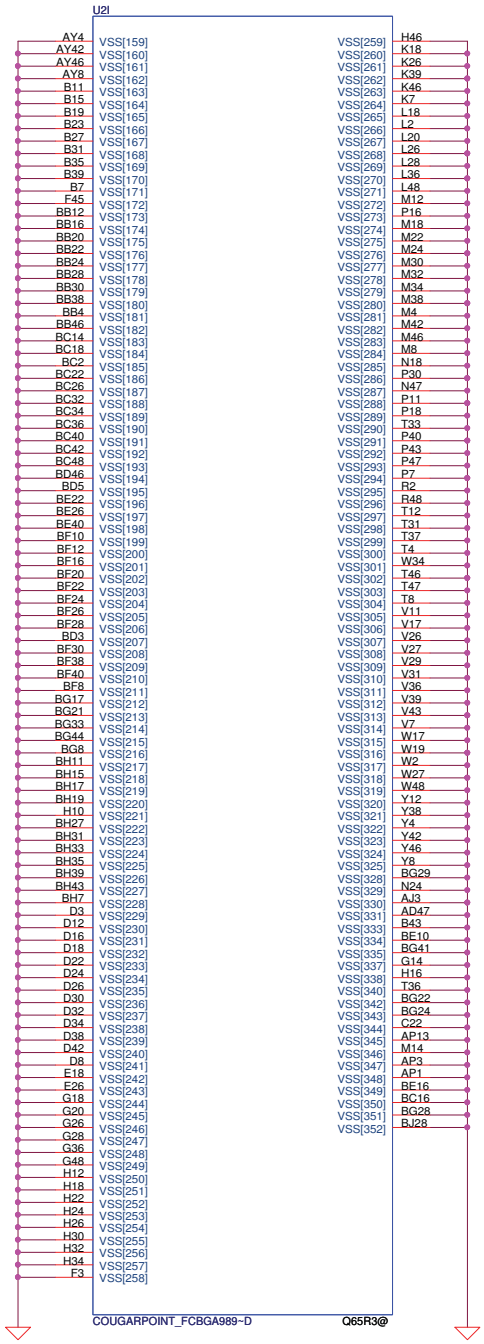

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Compal Electronics, Inc.

Title: ***PCH_GND***

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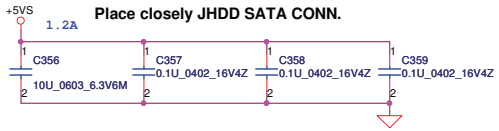
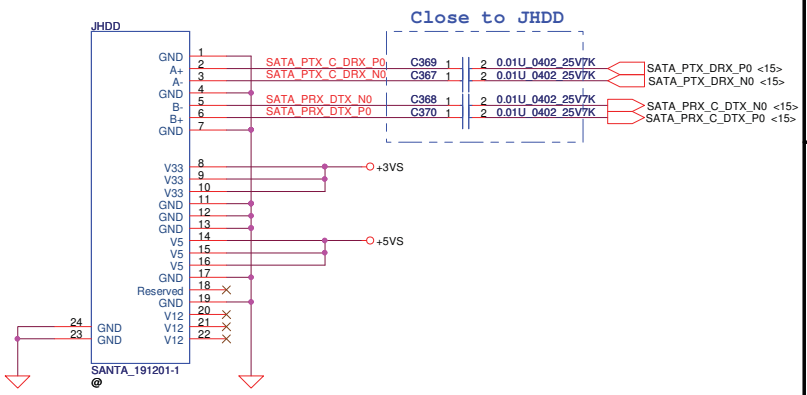
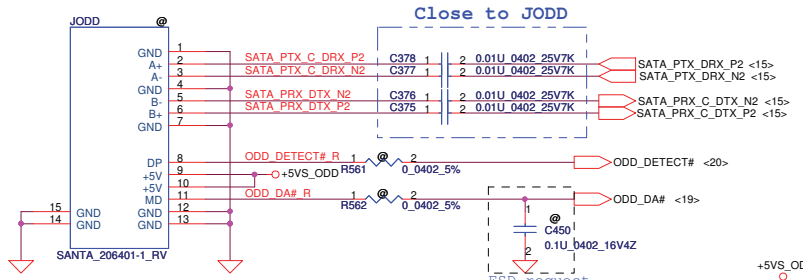
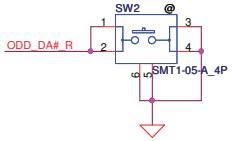


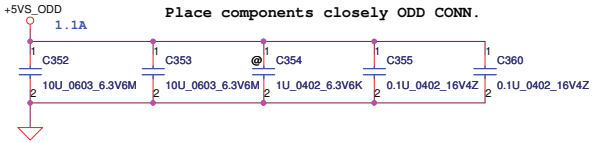
SATA HDD Conn.



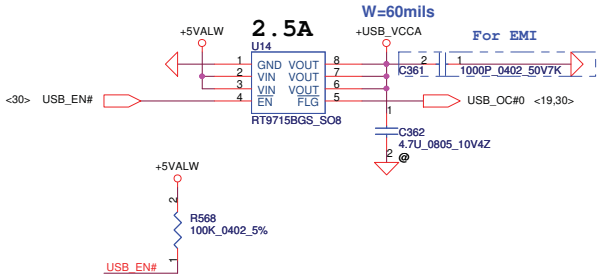
SATA ODD Conn

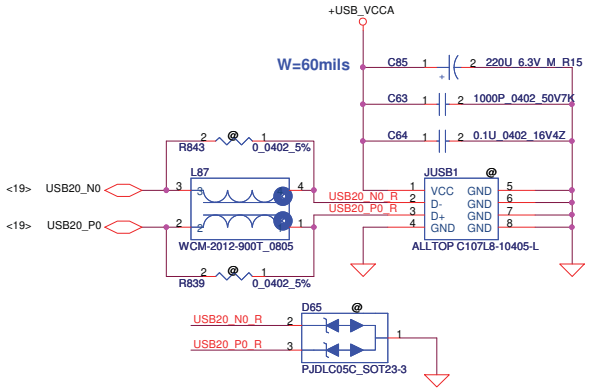


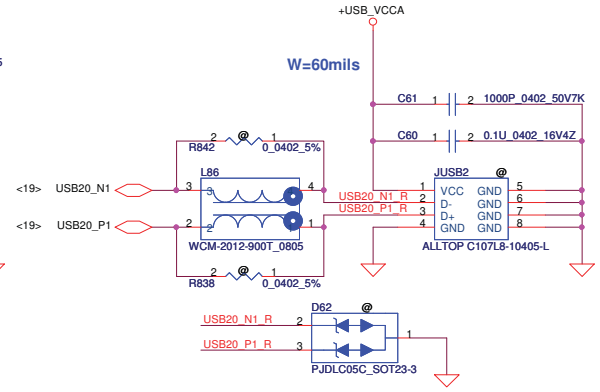




USB Conn. Left Side







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Compal Electronics, Inc.

Title: **SATA-HDD/ODD/USB**

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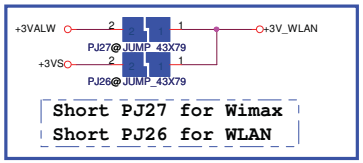
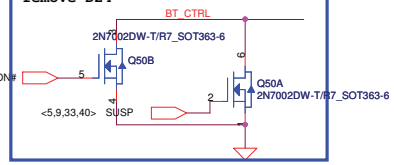
Slot 1 Half PCIe Mini Card-WLAN/ WiMax

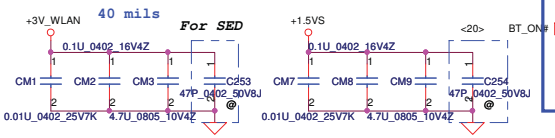


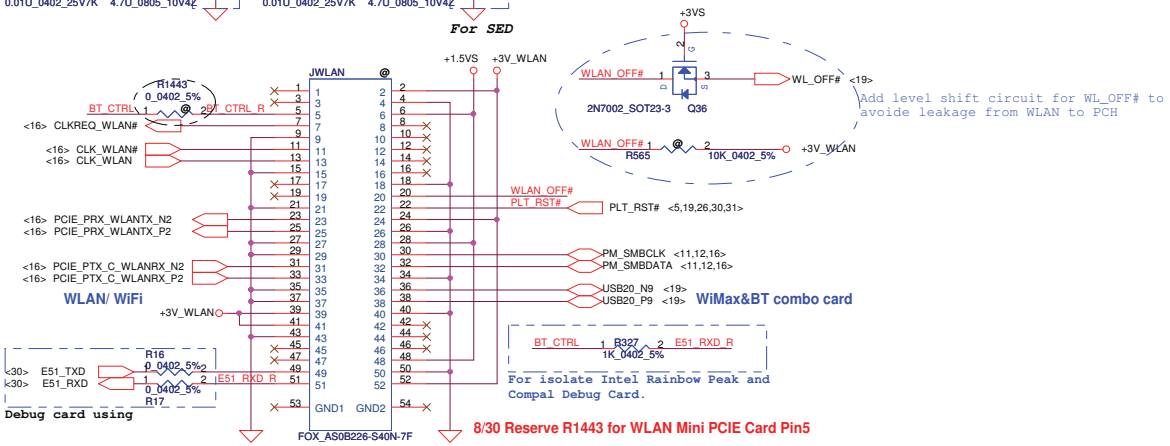
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24







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Compal Electronics, Inc.

Title: PCIe-WLAN

Size | Document Number: PWWHA LA-7202P M/B | Rev: 1.0

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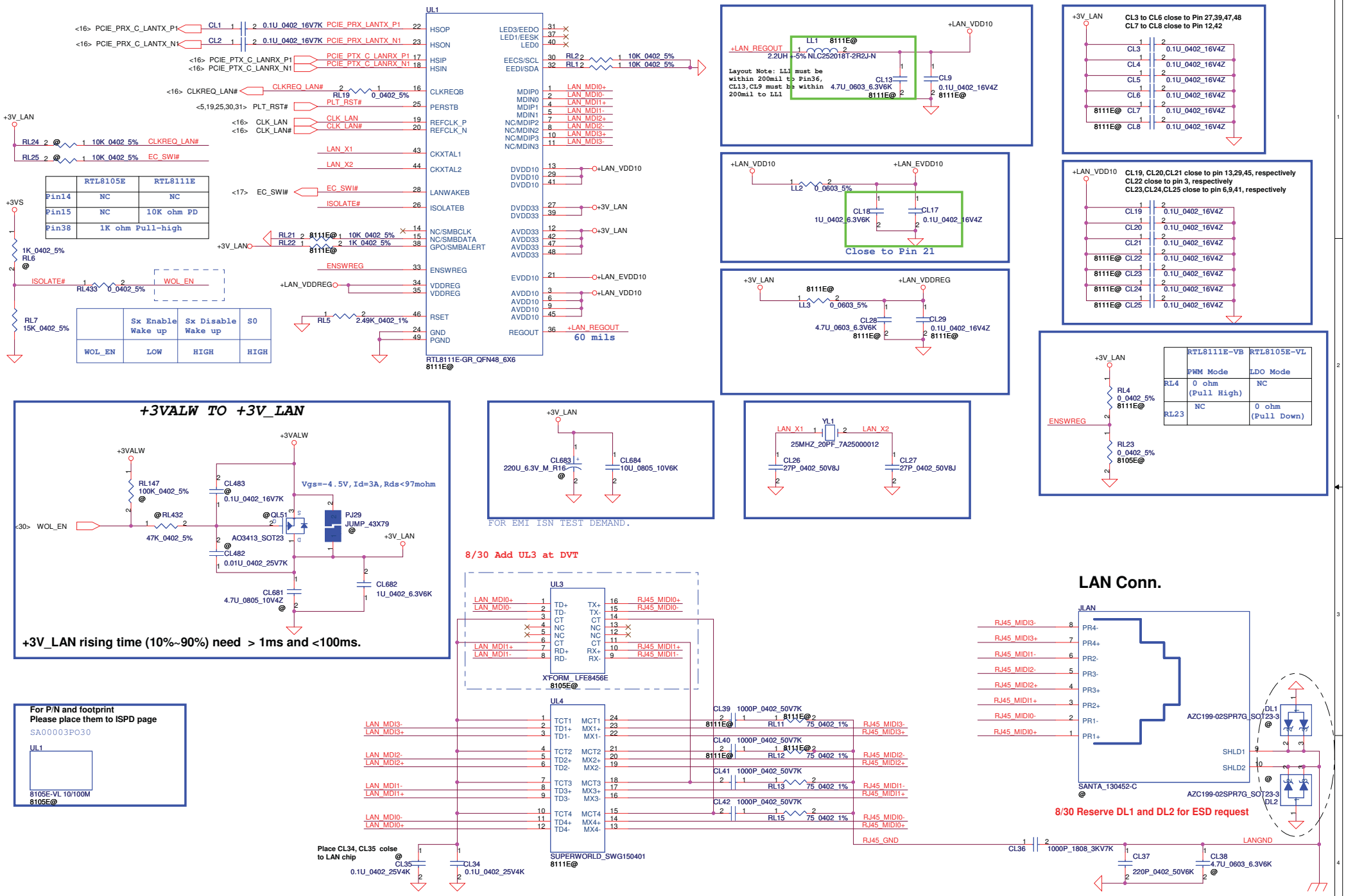

	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN	LOW	HIGH	HIGH

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Title: PCIe-LAN-RTL8105E/8111E

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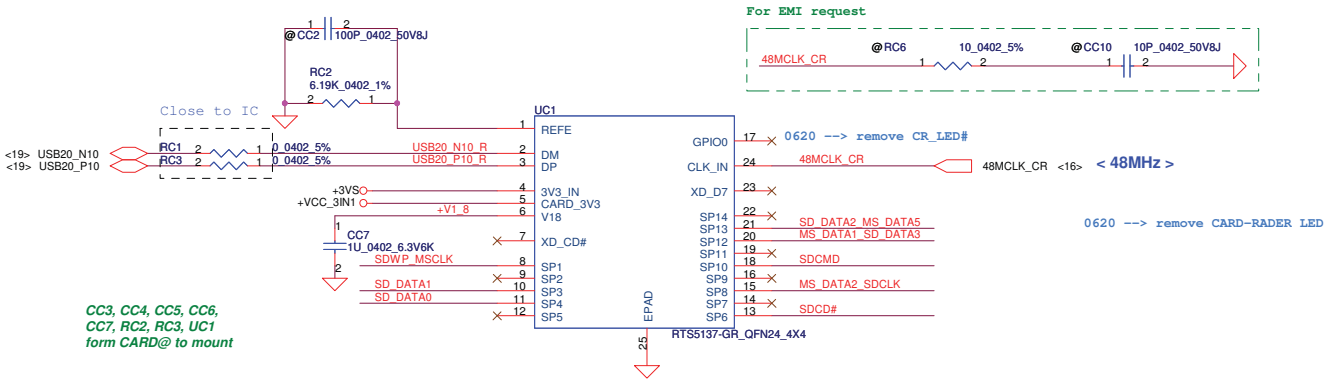
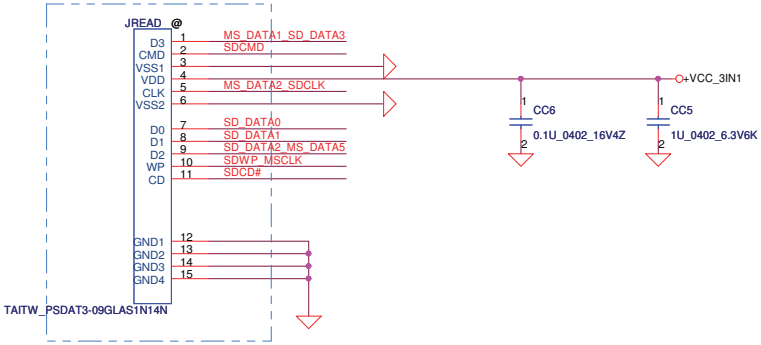


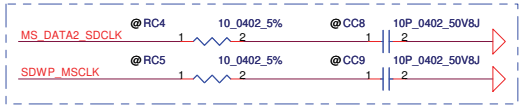
0715 --> change P/N to RTS5137 (SA000043500)

< 2 in 1 Card Reader >

0624 --> change CARDREADER conn.



For EMI request



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Compal Electronics, Inc.

Title: PCIe-CardReader RTS5137

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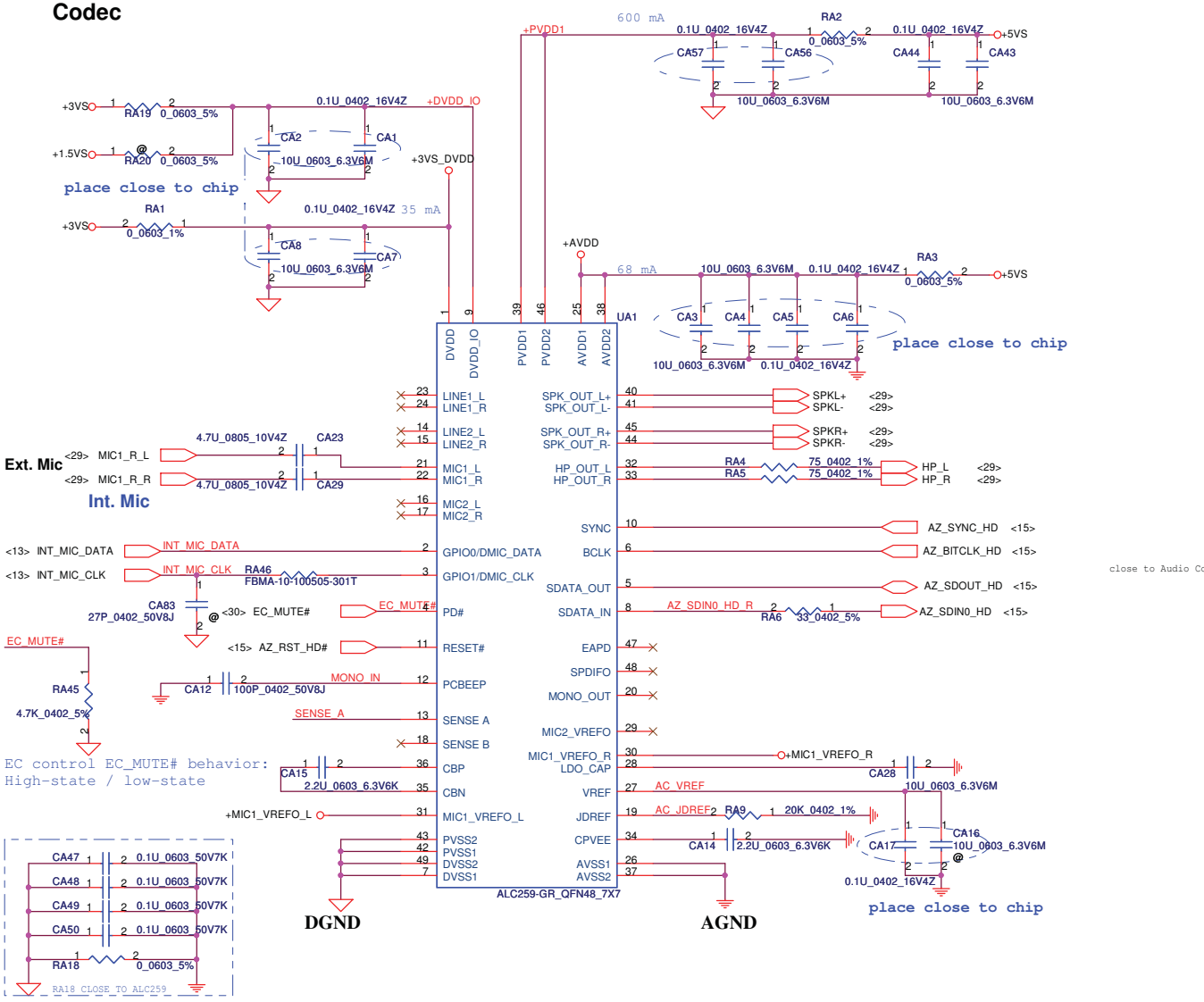
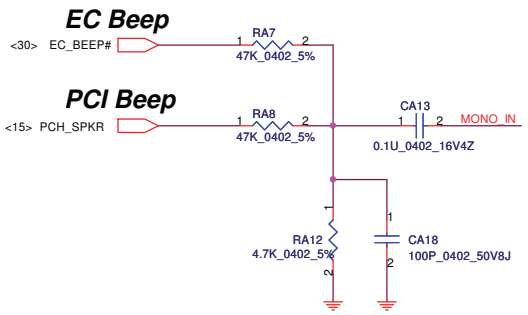
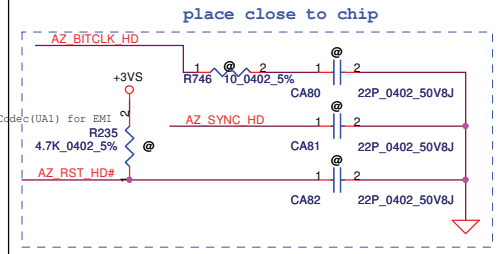
Codec

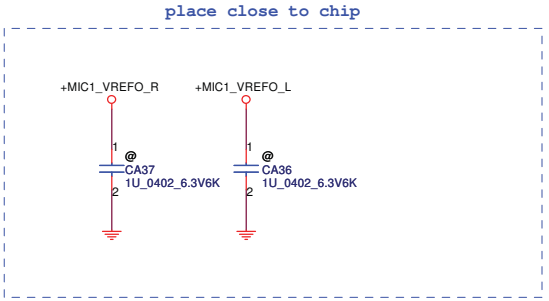


Beep sound

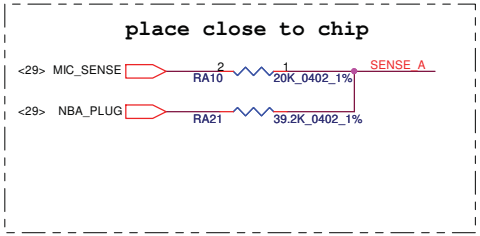




close to Audio Codec(UA1) for EMI



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



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Title: HDA-ALC259

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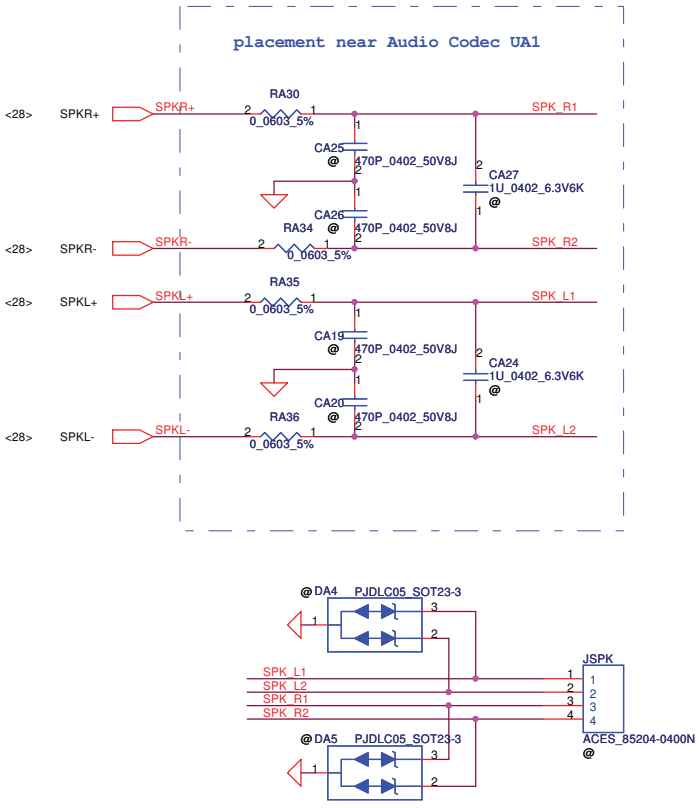
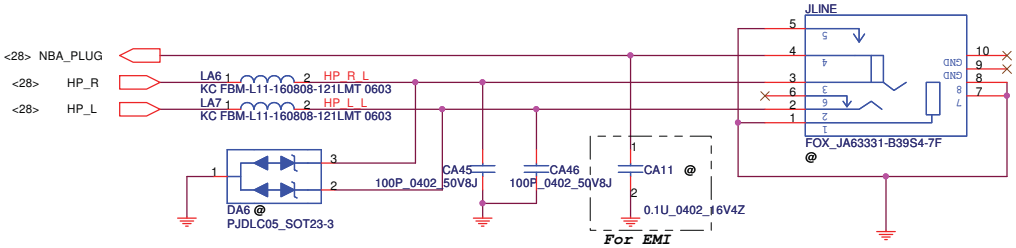
Speaker Connector

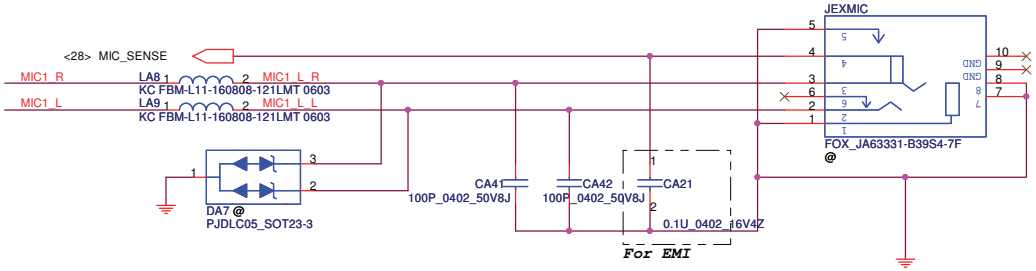


Ext. Mic

HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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Compal Electronics, Inc.

Title: AUDIO AMP/MIC/SPK/VR

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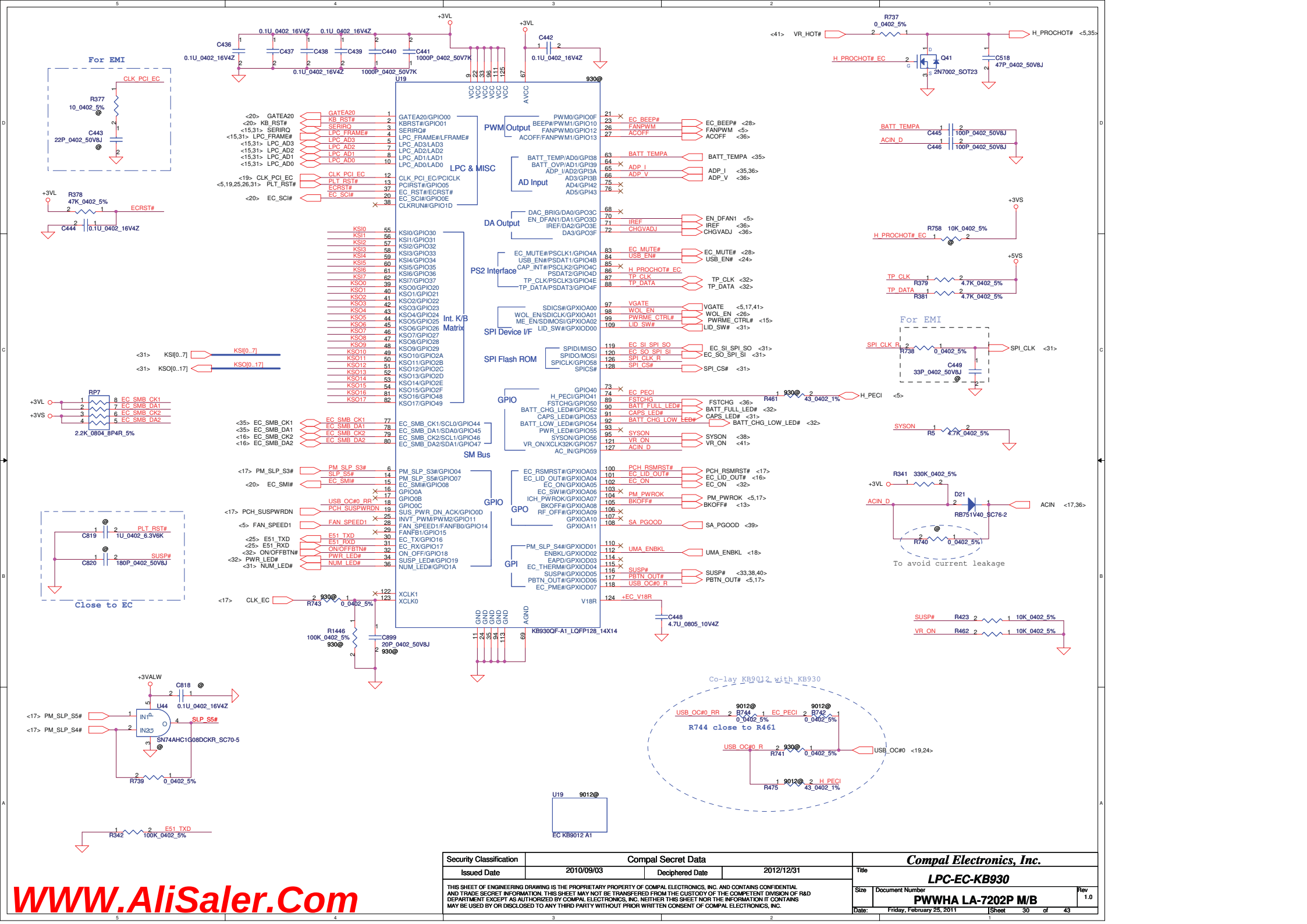

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Title: **LPC-EC-KB930**

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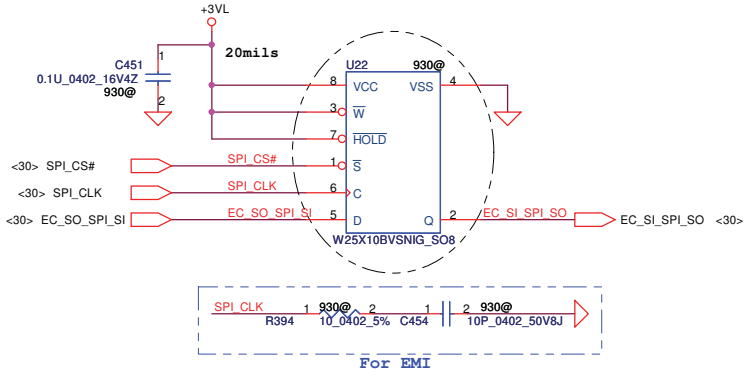
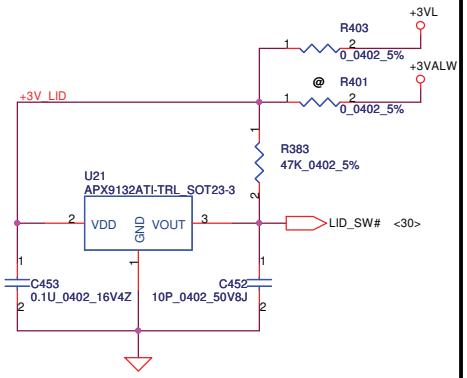
SPI Flash (256KB)

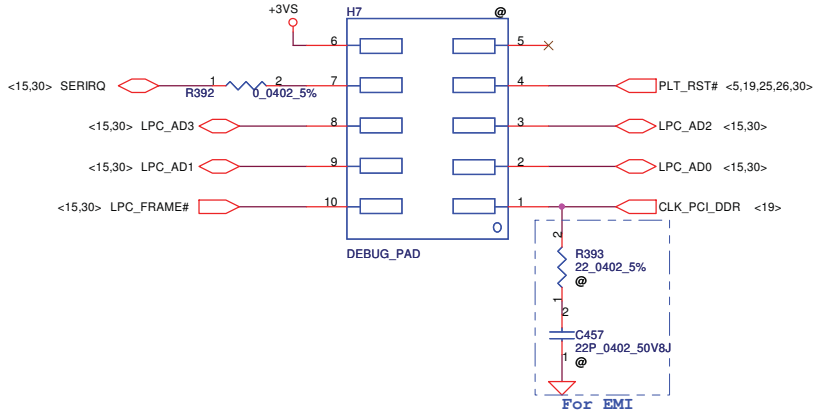


Lid SW

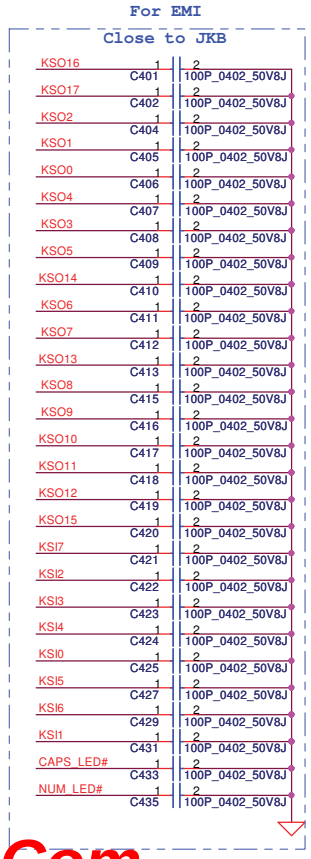


LPC Debug Port

Place the PAD under DDR DIMM.



KEYBOARD CONN.



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Compal Electronics, Inc.

Title: SPI ROM/LID/Debug/KB

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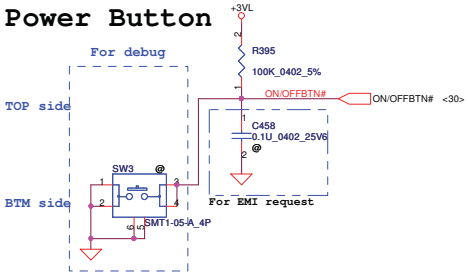
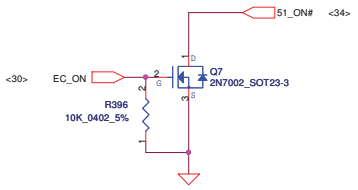
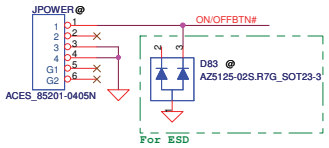
Power Button

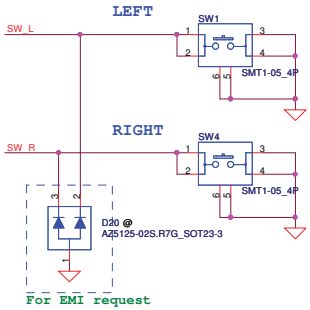


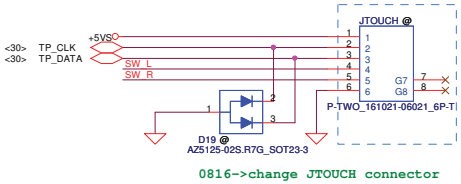


PWR/B to MB Conn.

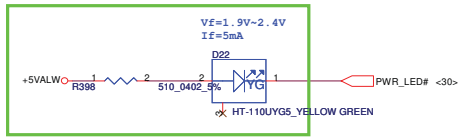


TP Button/Conn.

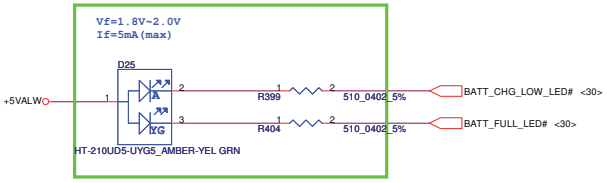




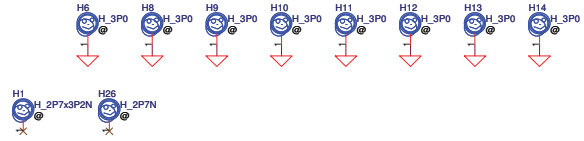
POWER/SUSPEND LED

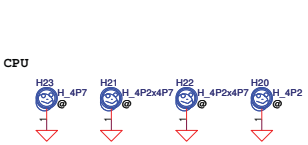


BATT CHARGE/FULL LED



Screw Hole





PCB Fedical Mark PAD

ISPD

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Compal Electronics, Inc.

Title: **PWR&TP CON/LED/ISPD**

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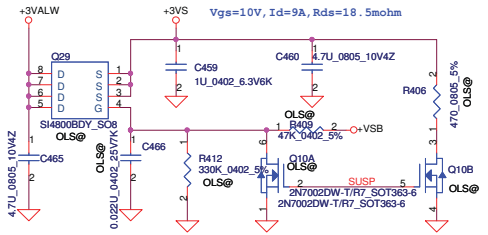
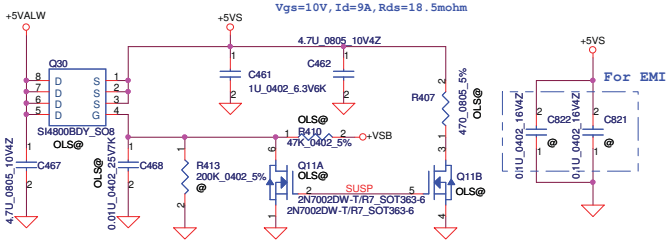
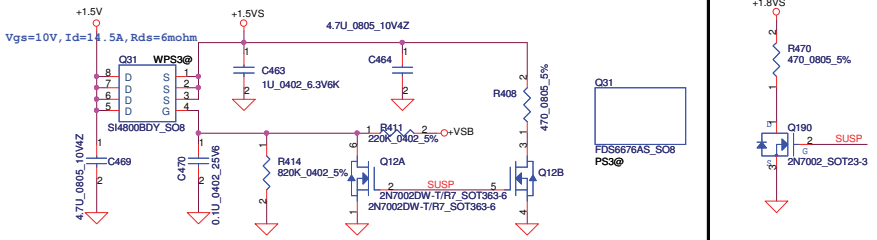
+3VALW TO +3VS



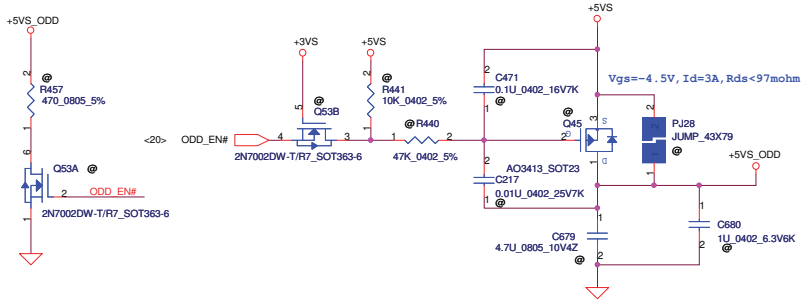
+5VALW TO +5VS



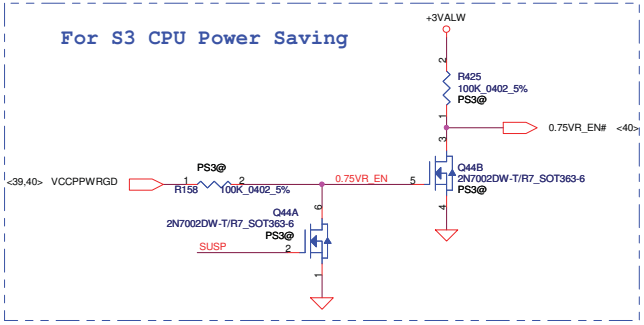
+1.5V to +1.5VS

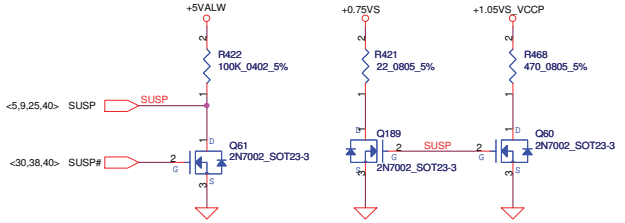


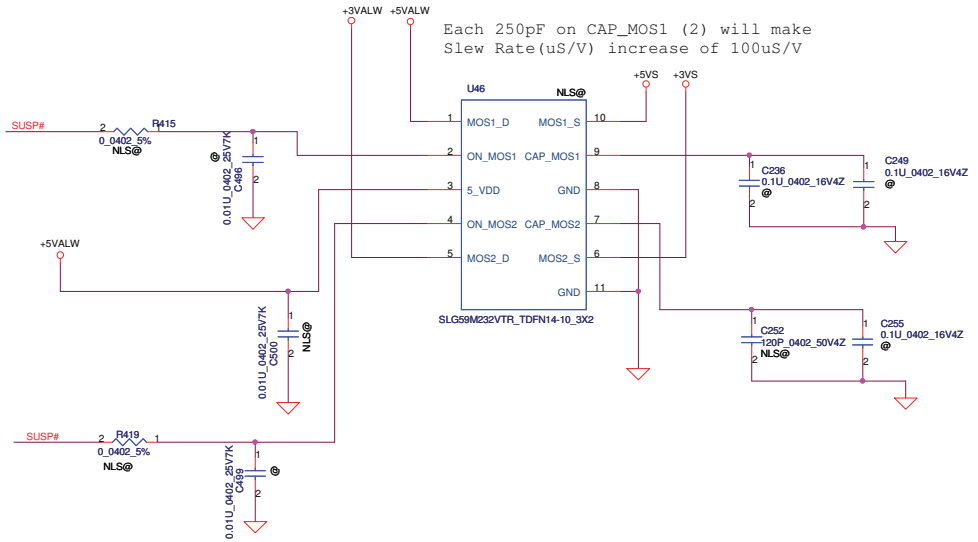
+5VS TO +5VS_ODD



For S3 CPU Power Saving







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Title: DC-DC INTERFACE

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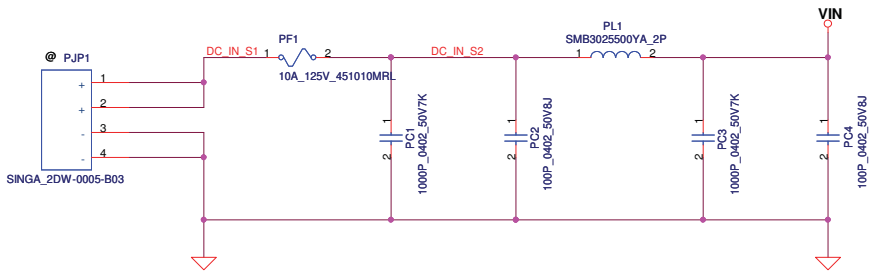
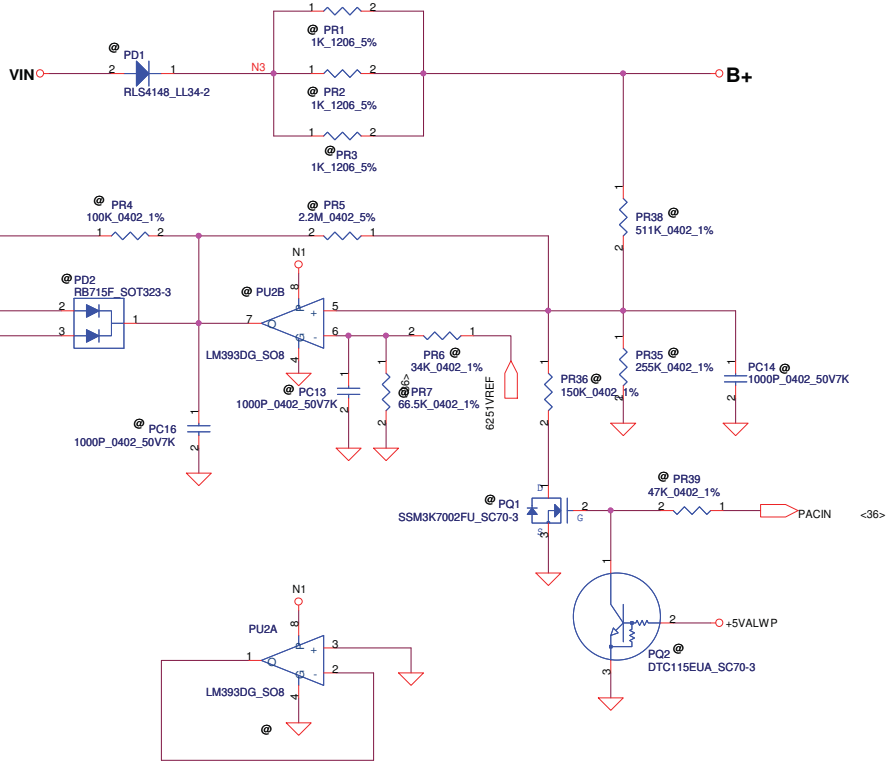
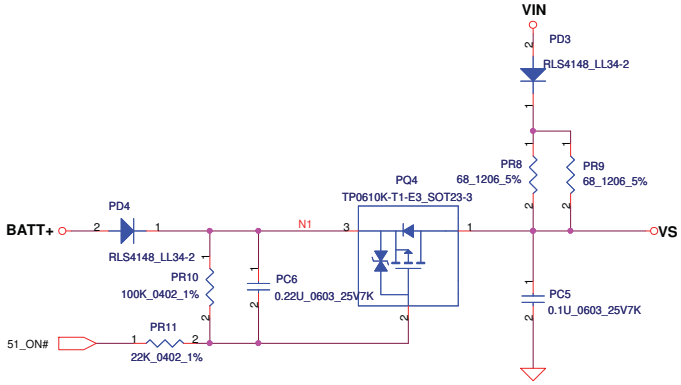
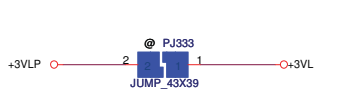


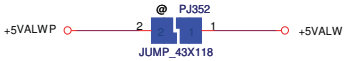






(100mA,40mils ,Via NO.= 2)

(5A,200mils ,Via NO.= 10)
OCP=8.6A



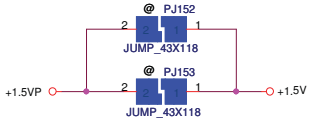
(5A,200mils ,Via NO.= 10)
OCP=7.9A

(120mA,40mils ,Via NO.= 1)

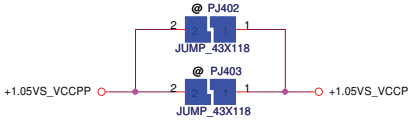
(1.65A,70mils ,Via NO.= 4)
OCP=4.2A

(1A,40mils ,Via NO.= 2)

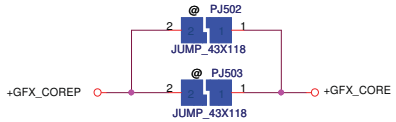
(6A,240mils ,Via NO.= 12)



(16A,640mils ,Via NO.= 32)



(17A,680mils ,Via NO.=34)



(33A,1320mils ,Via NO.=66)
OCP=40A

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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Compal Electronics, Inc.

Title: ***DCIN/VIN DECTOR***

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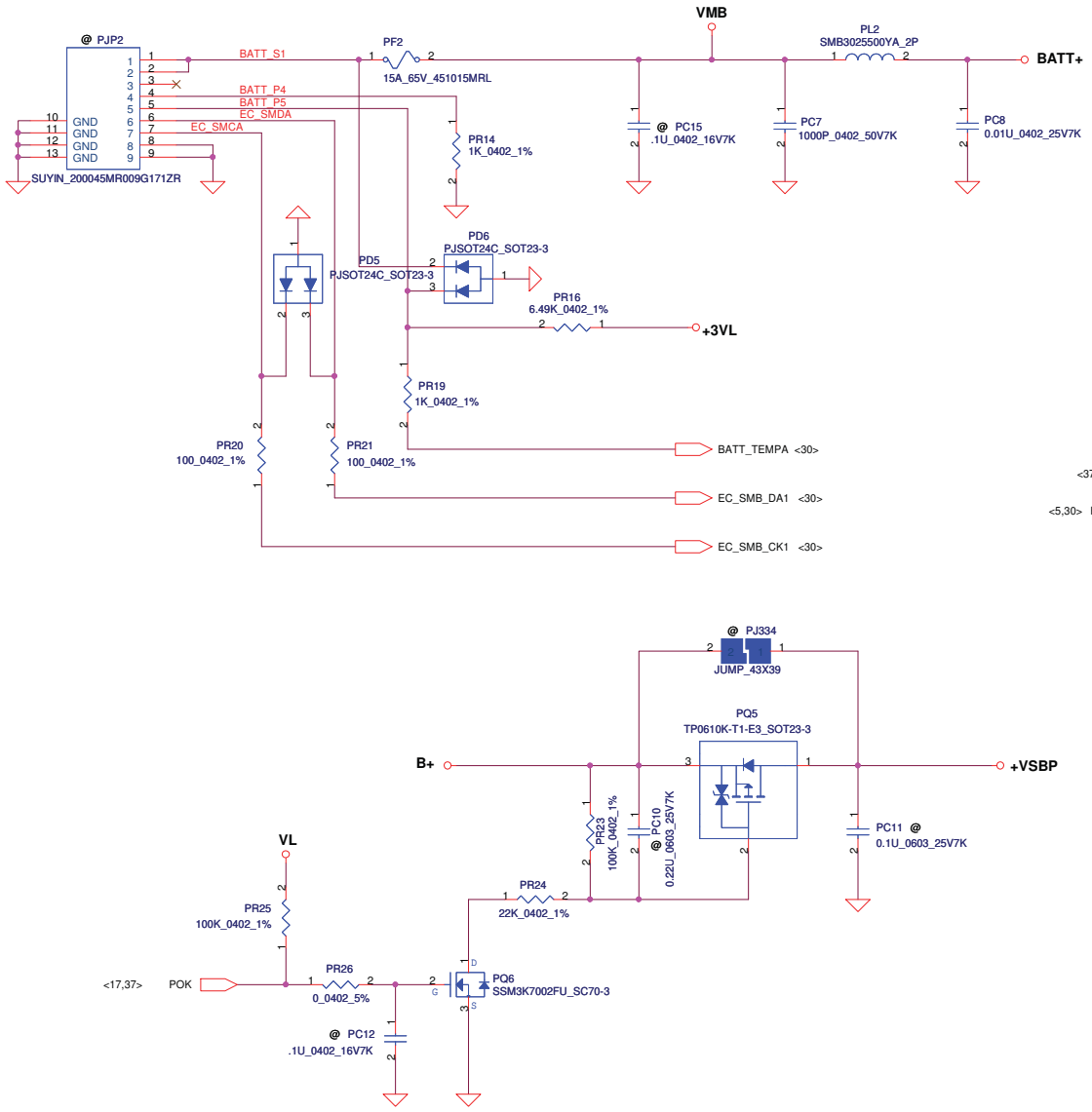
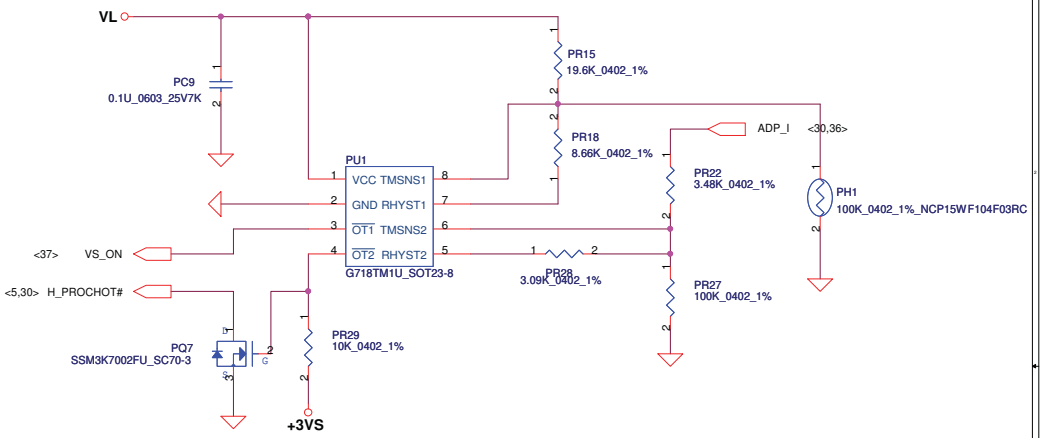


PH1 under CPU botten side :

CPU thermal protection at 95 degree C

Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V

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Title: ***BATTERY CONN / OTP***

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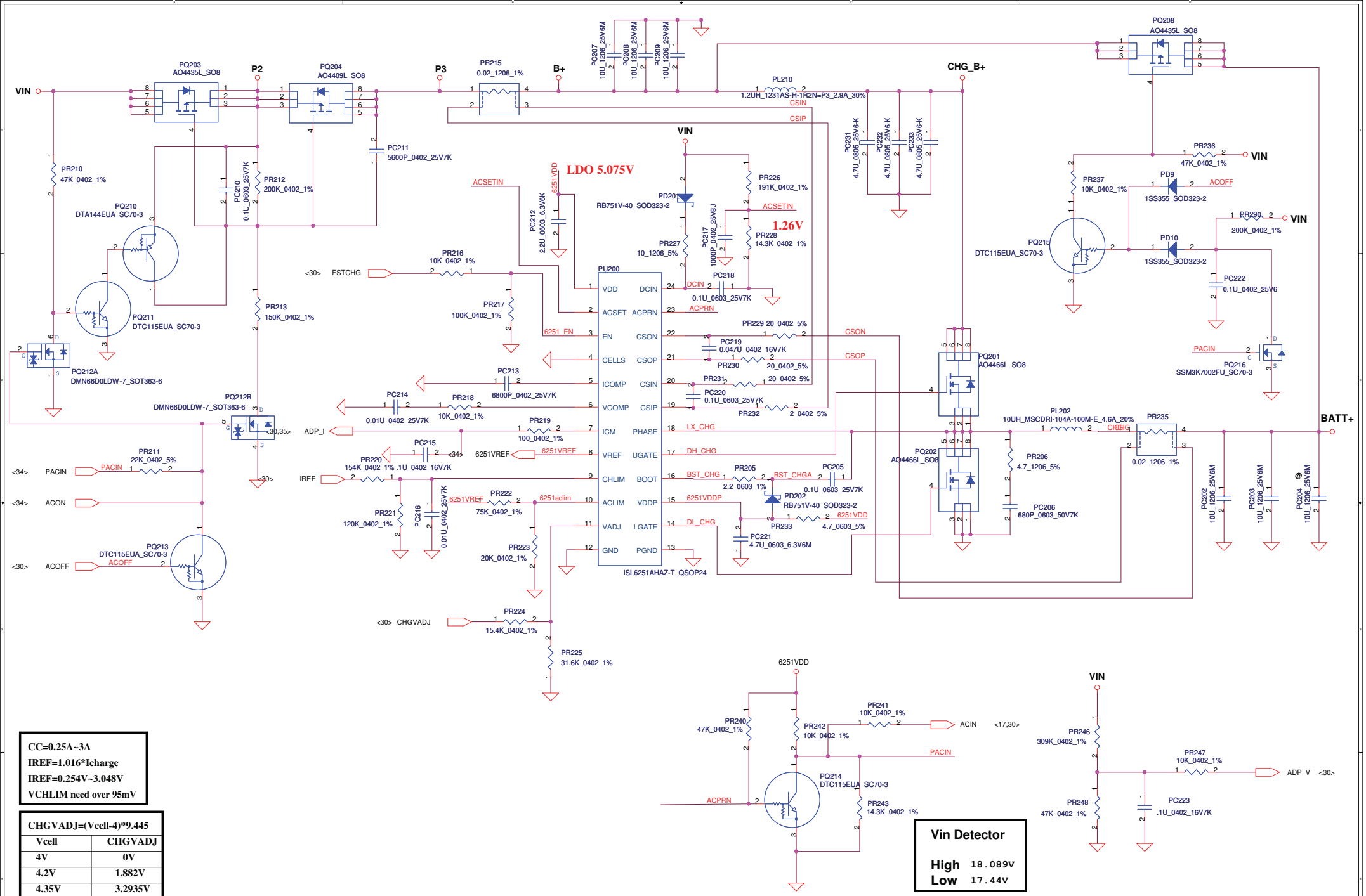

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode

Iada=0~3.42A(65W) CP= 92%*Iada; CP=3.147A
Vaclim=1.08V(65W) PR222=75k PR223=20k PR215=0.02
Iada=0~3.947A(75W) CP= 92%*Iada; CP=3.63A
Vaclim=1.35V(75W) PR222=75k PR223=20k PR215=0.02

Vin Detector

High 18.089V
Low 17.44V

1.26 / 14.3 * 205.3 = 18.089V

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Compal Electronics, Inc.

Title: **CHARGER**

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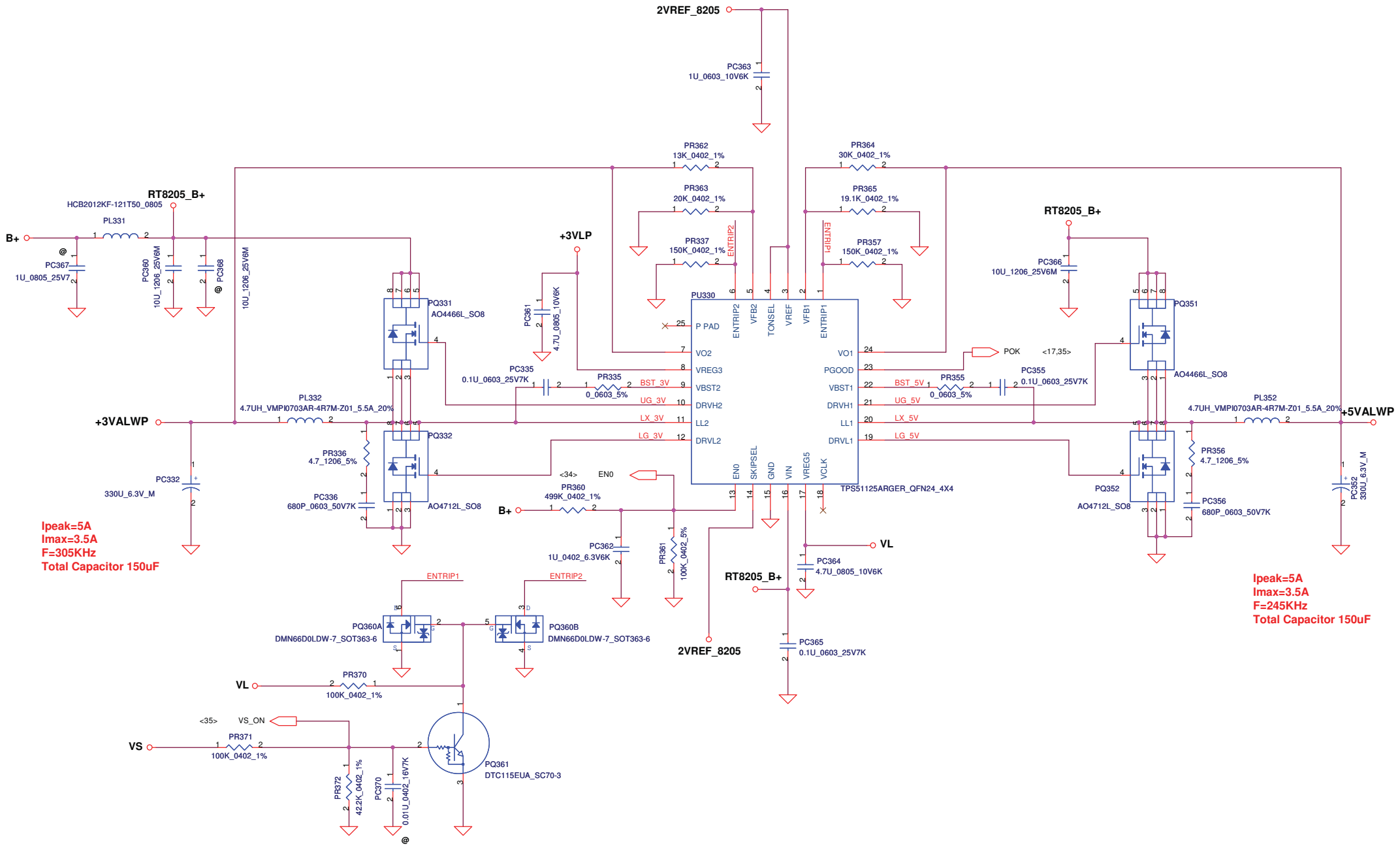

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Title: *3VALWP/5VALWP*

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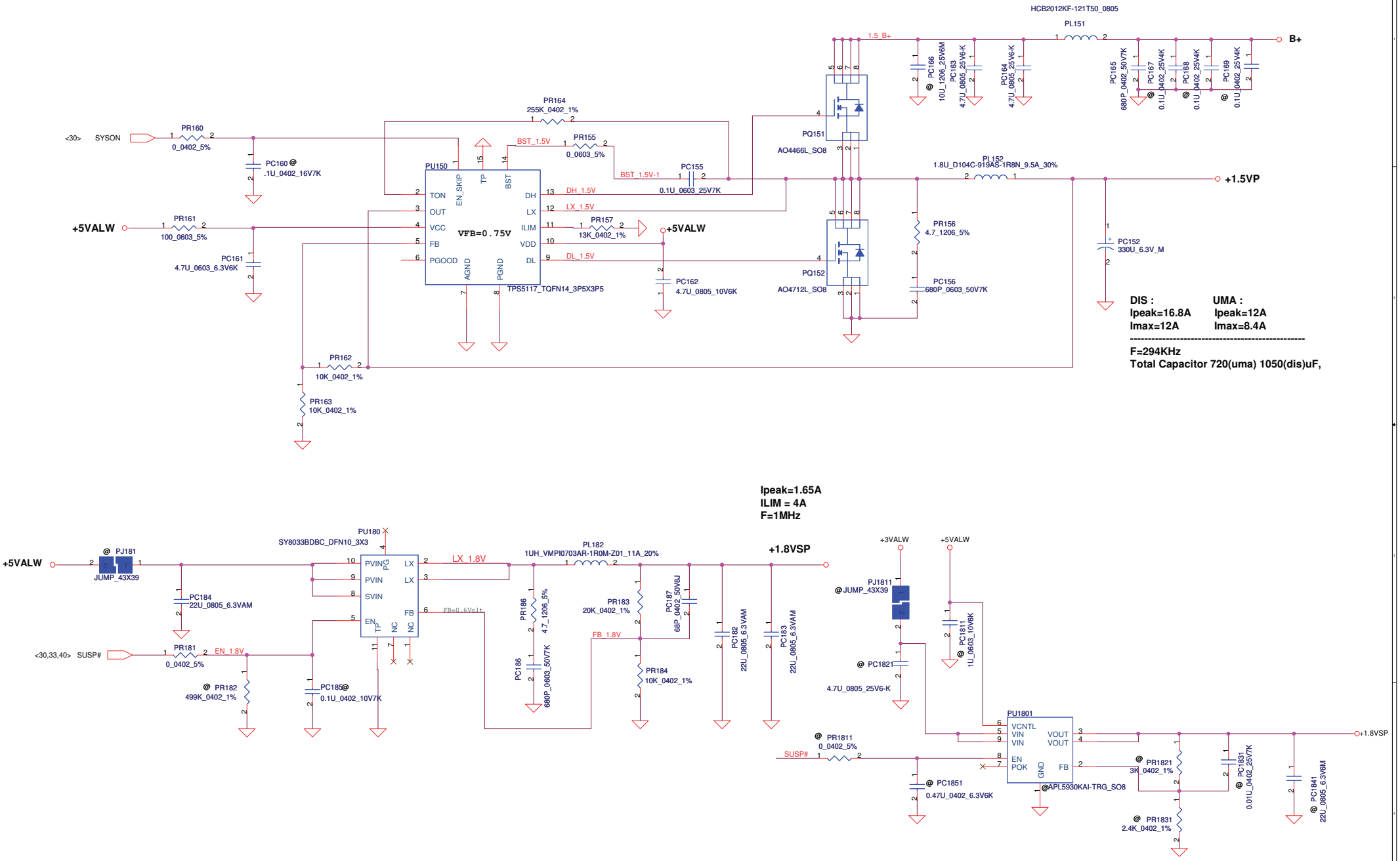

Security Classification	Compal Secret Data		
Issued Date	2010/09/03	Deciphered Date	2012/12/31

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Title: *+1.5VP/+1.8VSP*

Size	Document Number	Rev
Custom	PWWHA LA-7202 M/B	1.0

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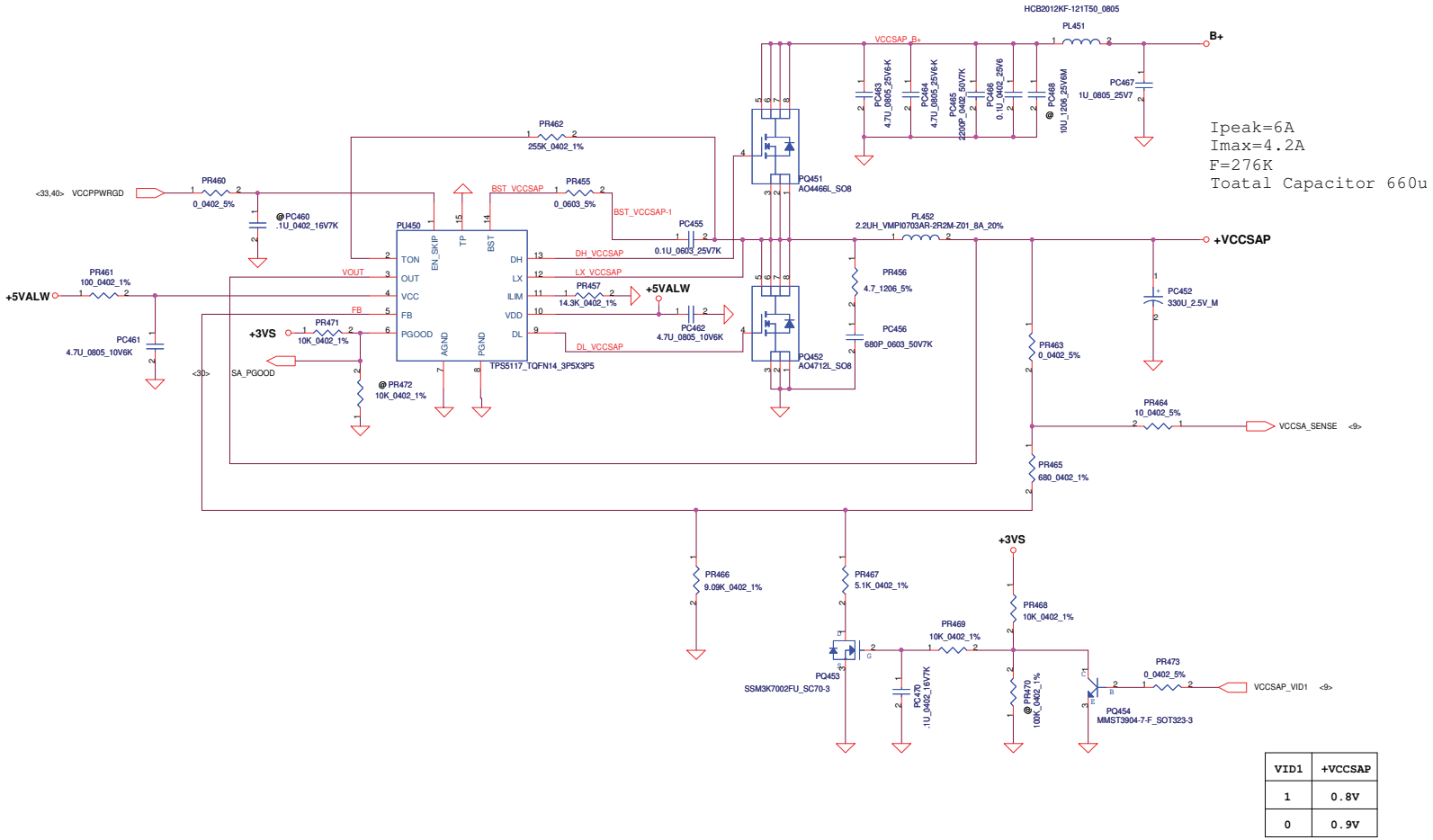

VID1	+VCCSAP
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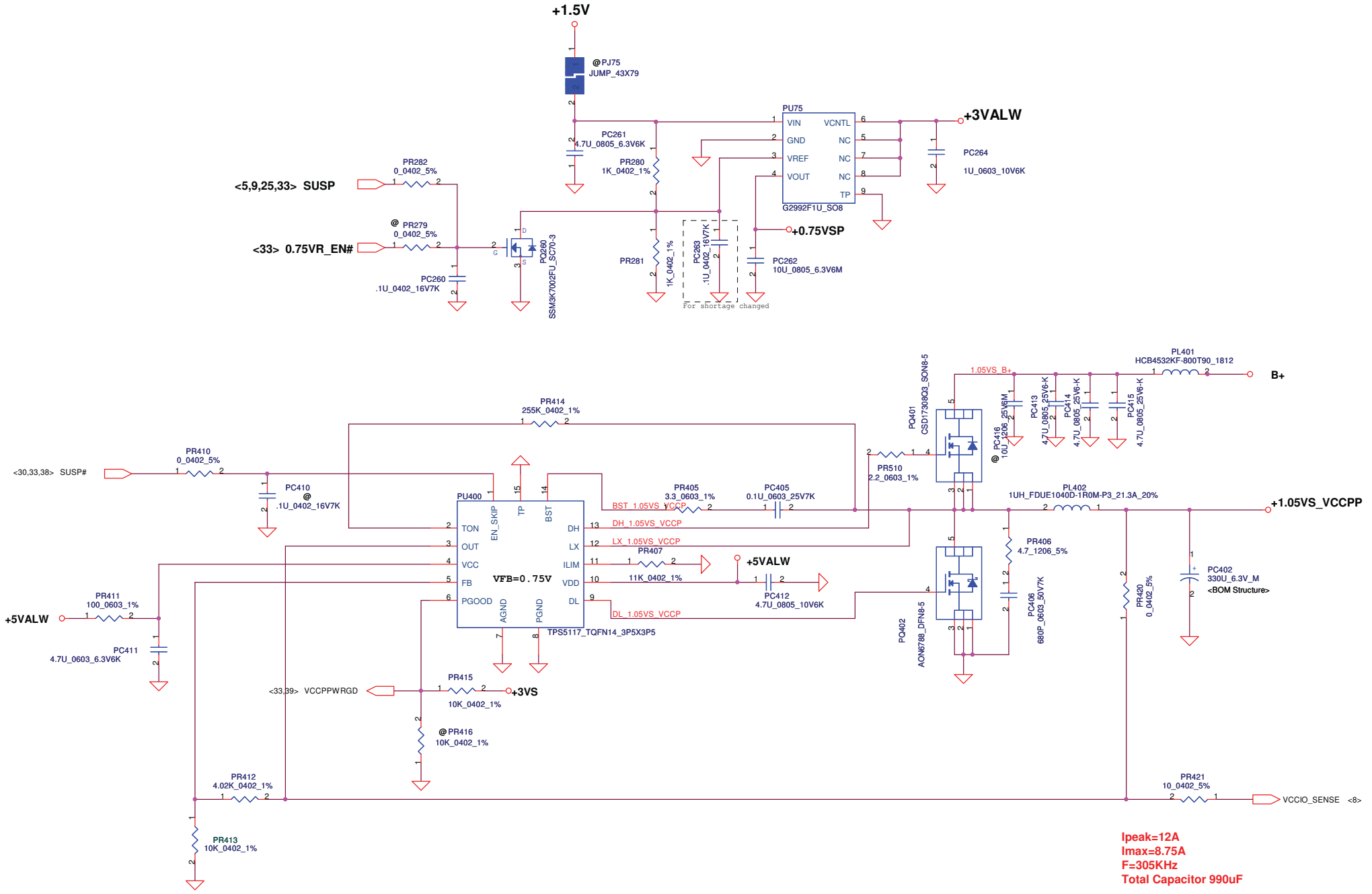

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Title: +1.05VS_VCCP/+0.75VSP

Size	Document Number	Rev
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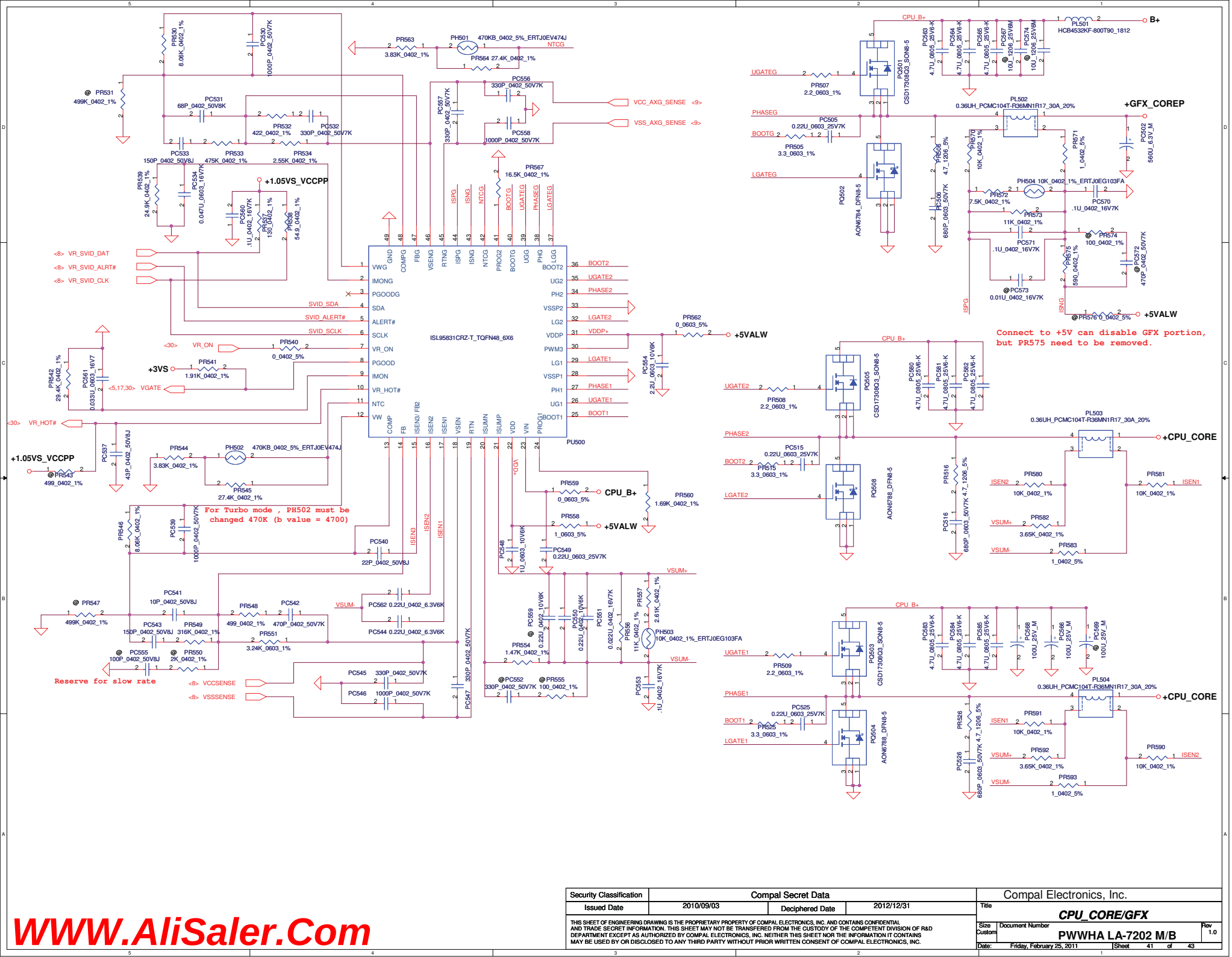

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Title: **CPU_CORE/GFX**

Size	Document Number	Rev
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PAGE	MODIFICATION LIST	PURPOSE
2010/12/31(PVT) P36 Charger	Change PQ203,PQ208 to AO4435L	Cost down
2010/12/31(PVT) P36 Charger	add PQ207,PQ208,PQ209 10u	EMI command
2010/12/31(PVT) P36 Charger	add snubber PR206,PC206	EMI command
2010/12/31(PVT) P36 Charger	change boost to 2.2 ohm PR205	EMI command
2010/12/31(PVT) P35 +3VALW/+5VALW	add snubber PR336,PC336,PR356,PC336	EMI command
2010/12/31(PVT) P37 +1.5VP/+1.8VSP	add snubber PR156,PC156	EMI command
2010/12/31(PVT) P37 +1.5VP/+1.8VSP	add PC165 for MEI	EMI command
2010/12/31(PVT) P37 +VCCSA	add snubber PR456,PC456	EMI command
2010/12/31(PVT) P37 +VCCSA	change output capacitor PC452 to OS-con	cost down
2010/12/31(PVT) P37 +VCCSA	change choke PL452 to molding	cost down
2010/12/31(PVT) P38 +1.05VS/+0.75	add snubber PC406 PR406	EMI command
2010/12/31(PVT) P38 +1.05VS/+0.75	change 0.75V enable PR279 tp PR282	HW command
2010/12/31(PVT) P39 +CPU_CORE	change PC549,PC515,PC525,PC 505 to correct rating	design change
2010/12/31(PVT) P39 +CPU_CORE	change PL502,PL503,PL504 to DCR 5%	design change
2010/12/31(PVT) P39 +CPU_CORE	change PC568 PC 566 to 5.8mmm capacitor	design change
2010/12/31(PVT) P39 +CPU_CORE	change PL551 for load line adjust	design change
2010/12/31(PVT) P39 +CPU_CORE	change PR560 for program temperture	design change
2010/12/31(PVT) P39 +CPU_CORE	change PC502,PC531,PC532 for burn-in shun down	design change

Title: <Title>		
Size: A	Document Number: PWWHA LA-7202P M/B	Rev: 1.0
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HW PIR (Product Improve Record)

PWWHA LA-7202P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2011/02/18

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	01/24	05	modify FAN with BTO item PWM and RPM	For HW BTO item
2)	01/24	05	modify RPM FAN connector pin define	Request from thermal team
3)	02/14	30	co-lay KB9012	For BTO item
4)	02/15	24	Add C450	For ESD request

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Issued Date	2010/09/03	Deciphered Date	2012/12/31

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Title: *HW-PIR*		
Size: Custom	Document Number: PWWHA LA-7202P M/B	Rev: 1.0
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